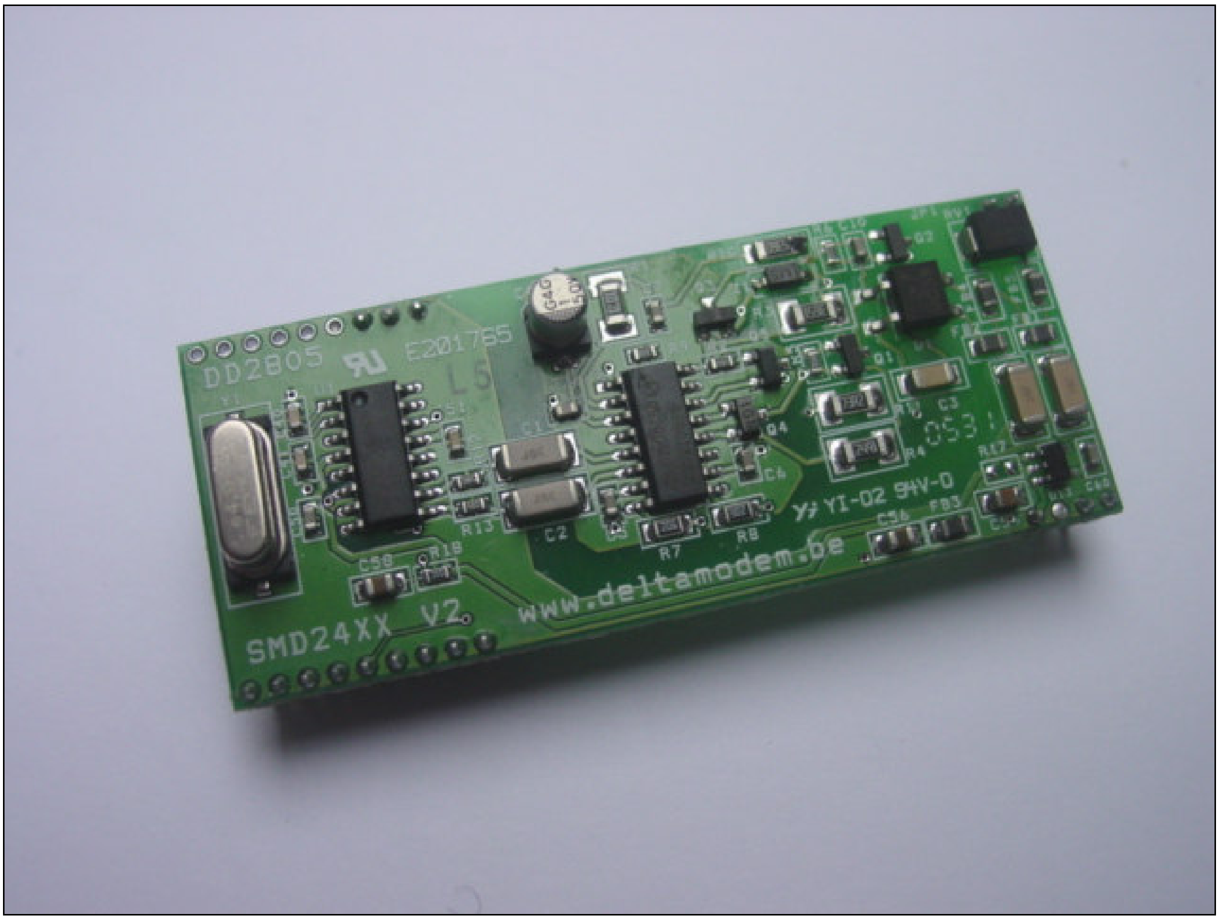
SMD24XXL

MODEM MODULE MANUAL



DocNumber:	**SMDXXL_MANUAL**	DELTA DESIGN
Version:	181105	
VersionDate:	18/11/2005	

Copyright Delta Design BVBA

TABLE OF CONTENTS

Copyright Delta Design BVBA

Copyright Delta Design BVBA

Copyright Delta Design BVBA

1 INTRODUCTION

1.1 PURPOSE

This document describes the SMD24XXL MODEM MODULE.
The SMD24XXL MODEM MODULE is a complete modem module that meets global telephone line requirements. Available in a socket (64,5 mm x 26,5mm) size footprint, the device is ideal for embedded modem applications due to its small board space, low power consumption and global compliance. The device is available in 5 different versions, ranging from V.92 down to V.22bis. Each version is available with in a 5V version and a 3V3 version.
The module allows you to reduce time to market by using a ready to use approved solution.

1.2 VERSIONS

ORDERING INFORMATION	
SMD2404L-3V3	V.22bis modem 3V3 supply
SMD2404L-5V	V.22bis modem 5V supply
SMD2415L-3V3	V.32bis modem 3V3 supply
SMD2415L-5V	V.32bis modem 5V supply
SMD2434L-3V3	V.34 modem 3V3 supply
SMD2434L-5V	V.34 modem 5V supply
SMD2457L-3V3	V.90 modem 3V3 supply
SMD2457L-5V	V.90 modem 5V supply
SMD2493L-3V3	V.92 modem 3V3 supply
SMD2493L-5V	V.92 modem 5V supply

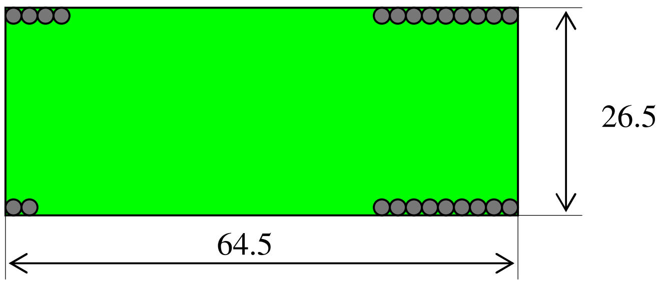
1.3 GENERAL MODEM FEATURES

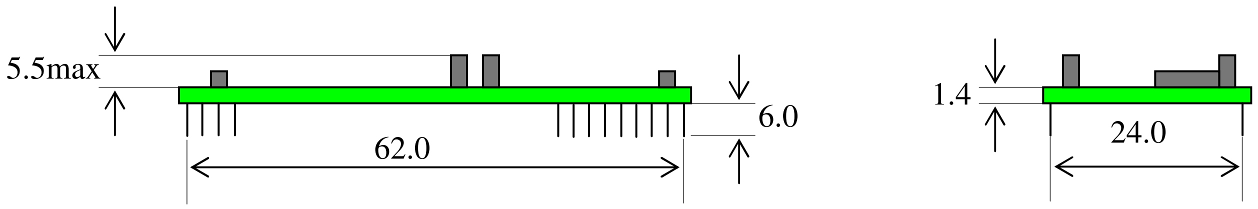
Feature	SMD2404L	SMD2415L	SMD2434L	SMD2457L	SMD2493L
Max line Speed(bps)	2400/2400	14400/14400	33600/33600	33600/56000	48000/56000
ITU V.42 MNP2-4	X	X	X	X	X
ITU V.42bis MNP5		X	X	X	X
ITU V.44					X
Fast Connect V.21/V.22/V.29	X	X	X	X	X
Ring detector	X	X	X	X	X
Overvoltage protection	X	X	X	X	X
Autodial DTMF	X	X	X	X	X
Pulse Dial	X	X	X	X	X
Autoanswer	X	X	X	X	X
ITU V.21	X	X	X	X	X
ITU V.22	X	X	X	X	X
ITU V.22bis	X	X	X	X	X
ITU V.32		X	X	X	X
ITU V.32bis		X	X	X	X
ITU V.34			X	X	X
ITU V.90				X	X
ITU V.92					X

Copyright Delta Design BVBA

2 PHYSICAL DIMENSIONS

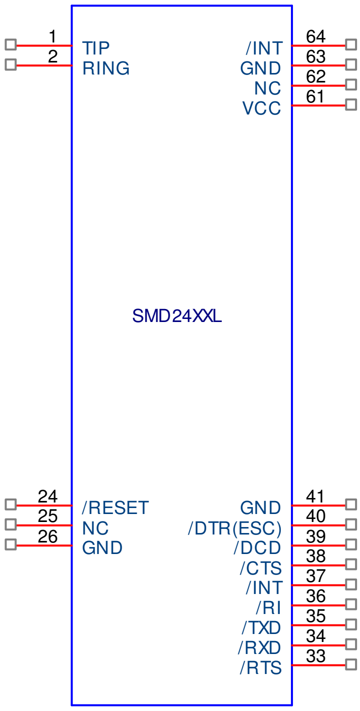
All Dimensions in mm
Length : 64.5 ± 0.2 mm
Width : 26.5 ± 0.2 mm
Pin pitch : 2 mm





Copyright Delta Design BVBA

3 INTERFACE



3.1 PIN DESCRIPTION

PIN	NAME	DESCRIPTION	Type
1	TIP	Telephone Line TIP	Phone Line
2	RING	Telephone Line RING	Phone Line
24	/RESET	An active low input that is used to reset all control registers to a defined initialized state.	Input
25	NC	Not Connected	-
26	GND	GND	GND
33	/RTS	Request To Send	Input
34	/RXD	Receive Data	Output
35	/TXD	Transmit Data	Input
36	/RI	Ring Indicator	Output
37	/INT	Interrupt output	Output
38	/CTS	Clear To Send	Output
39	/DCD	Data Carrier Detect	Output
40	/DTR (ESC)	Data Terminal Ready	Input
61	VCC	Vcc Power Supply (5V or 3V3)	POWER
62	NC	Not Connected	-
63	GND	GND	GND
64	/INT	Interrupt output	Output

3.2 DC CHARACTERISTICS

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.8	V
High Level Output Voltage	V_{OH}	I_O = -2mA	2.4	-	-	V
Low Level Output Voltage	V_{OL}	I_O = 2mA	-	-	0.35	V
Input Leakage Current	I_L		-10	-	10	µA

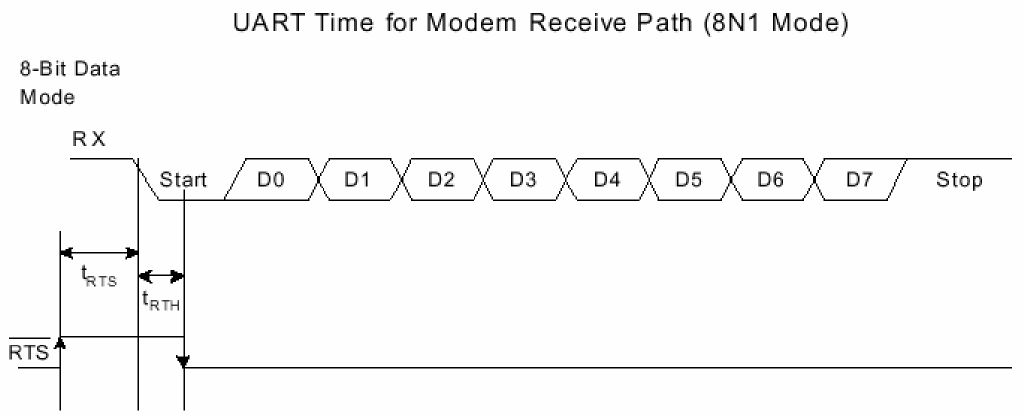
Copyright Delta Design BVBA

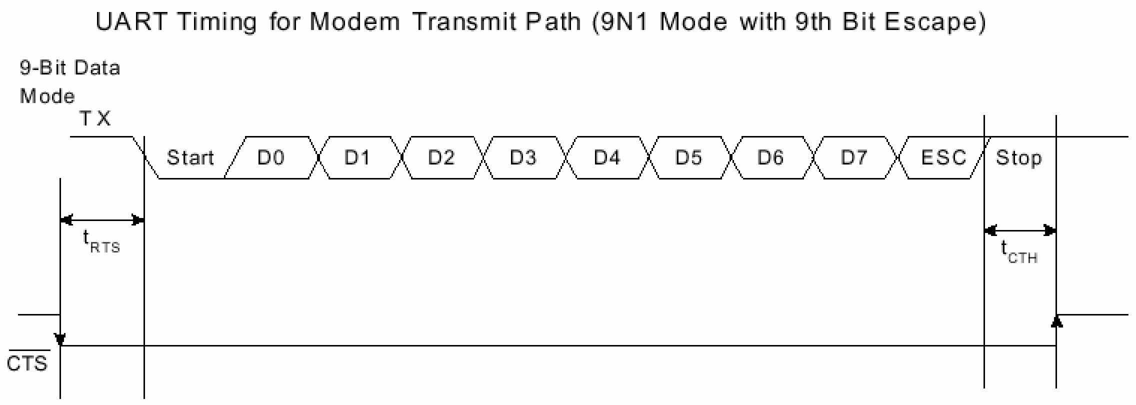
3.3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Current, SMD2493/57/34/15/04L Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	-0.3 to 5.3	V
Operating Temperature Range	T_A	-10 to 100	°C

3.4 SWITCHING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Baud Rate Accuracy	t_{BD}	-1	-	+1	%
Start Bit ↓ to /RTS ↓	t_{RTH}	-	1/(2x Baud Rate)	-	ns
/CTS or /RTS ↑ High to start Bit ↓	t_{RTS}	10	-	-	ns
Stop Bit ↑ to /CTS ↑	t_{CTH}	-	-	-	ns
/RESET ↓ to /RESET ↑	t_{RS}	5.0	-	-	ms
/RESET ↑ to 1st AT Command	t_{AT}	300	-	-	ms





3.5 POWER SUPPLY

3.3Vdc +-10%
Supply current : 35mA max
powerdown : 80uA typical
Wake-on-ring : 5mA max

Copyright Delta Design BVBA

4 OPERATION

4.1 FUNCTIONAL DESCRIPTIONI

The SMD24XXL is a complete modem module with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements.
The SMD24XXL accepts standard modem AT commands and provides connect rates up to 56 kbps full-duplex (SMD2493L, SMD2457L) over the Public Switched Telephone Network (PSTN). The SMD24XXL features a complete set of modem protocols including all ITU-T standard formats up to 56 kbps.
The SMD24XXL modem module provides numerous additional features for embedded modem applications. The modem includes full type I and type II caller ID detection and decoding for global standards. Call progress is supported through echoing result codes and is also programmable to meet global settings. Because the SMD24XXL modem module integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.
This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The SMD24XXL module includes a silicon DAA using Silicon Laboratories proprietary third-generation DAA technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the SMD24XXL has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, surge immunity, and safety requirements.
The SMD24XXL allows for rapid integration into existing applications by providing a serial interface that can directly communicate to either a microcontroller via a UART interface or a PC via an RS-232. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software.

The SMD24XXL includes an automatic baud rate detection feature that allows the host to start transmitting data at any standard DTE rate from 300 bps to 307.2 kbps. This feature is enabled by default.

4.2 COMMAND MODE

Upon reset, the SMD24XXL is in command mode and accepts “AT” commands. An outgoing modem call can be made using the “ATDT#” (tone dial) or “ATDP#” (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes and enters data mode.

4.3 DATA MODE

The SMD24XXL is in data mode while it has a telephone line connection to another modem or is in the process of establishing a connection.
In command and data mode, the SMD24XXL operates in asynchronous DTE mode only. Data protocols are available to provide error correction to improve reliability (V.44, V.42, and MNP2-4) and data compression to increase throughput (V.42bis and MNP5).
Each connection between two modems in data mode begins with a handshaking sequence. During this sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

4.4 FAST CONNECT

The SMD24XXL supports a fast connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, Bell103, and V.29 modulations. See 5.3 for details.

4.5 SYNCRONOUS ACCESS MODE

The SMD24XXL supports a synchronous access mode of operation, which operates with an asynchronous DTE and a synchronous DCE. See 5.4 for details.

4.6 LOW POWER/POWER DOWN

Using the S24 S-register, the SMD24XXL can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the TX FIFO has been empty. The modem remains in the sleep state until either a 1 to 0 transition on TXD occurs.
Additionally, the SMD24XXL may be placed in a complete powerdown mode or wake-on-ring mode. Complete powerdown is accomplished via U65[13] (PDN). Once the PDN bit is written, the SMD24XXL completely powers down and can only be powered back on via the RESET pin. See 5.7 for details.

4.7 DATA COMPRESSION

The modem can achieve DTE (host-to-modem) speeds greater than the maximum DCE (modem-to-modem) speed through the use of a data compression protocol. The compression protocols available are the ITU-T, V.44 (SMD2493L only) , V.42bis, and MNP5 protocols. Data compression attempts to increase throughput by compressing the data before actually sending it. Thus, the modem is able to transmit more data in a given period of time.
The SMD2404L does not support data compression.

Copyright Delta Design BVBA

4.8 ERROR CORRECTION

The SMD24XXL modem can employ error correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The modem supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

4.9 WIRE MODE

Wire mode is used to communicate with standard non-error correcting modems. When optioned with \N3, the SMD24XXL falls back to wire mode if it fails in an attempt to negotiate a V.42 link with the remote modem. Error correction and data compression are not active in wire mode.

4.10 V.92 PCM UPSTREAM(SMD2493L)

The SMD2493L supports the ITU-V.92 PCM upstream data protocol. This protocol allows the modem to connect at speed up to 48 kbps upstream. Previously the upstream connection rate was limited to 33.6 kbps. The PCM upstream mode is enabled by default; to disable, issue the AT command +PIG = 1 . To view both downstream and upstream connect speeds in the connect result message, issue the command “AT \V4” or “AT+MR”.

4.11 V.92 QUICK CONNECT(SMD2493L)

The SMD2493L supports the ITU-V.92 quick connect protocol. Quick connect enables the modem to save and reuse line condition parameters to reduce startup negotiation time.
The quick connect feature is enabled by default in the SMD2493L. For information on changing the quick connect settings, see the +PSS and +PQC commands.

4.12 V.92 MODEM-ON-HOLD(SMD2493L)

The modem-on-hold (MOH) feature allows the modem user to answer an incoming call while connected online without dropping the internet connection. The modem will remain “on hold” for a period of time determined by the host and the ISP. There are four AT commands that control the operation of MOH. The commands are as follows: +PCW, +PMH, +PMHT, +PMHR. By changing these parameters, the user can enable/disable call waiting and MOH, set the MOH request timeout, and set the MOH initiate timeout. The MOH feature is most useful when the SMD2493L is connected to a central office that allows call waiting.

4.13 CALLER-ID OPERATION

The SMD24XXL supports full type I and type II caller ID detection and decode. Caller ID is supported for the US Bellcore, European ETSI, UK, and Japanese protocols and is enabled via the +VCID, +VCDT, and +PCW commands.

4.14 PARALLEL PHONE DETECTION

The SMD24XXL is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the modem is using the phone line.

4.15 ON-HOOK LINE-IN-USE DETECTION

When the modem is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the modem to monitor the TIP-RING dc voltage with the line voltage sense (LVS) register (U66, bits 15:8). The LVS[7:0] bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed 2s complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING. See also the %Vn commands for automatic line-in-use detection.

4.16 OFF-HOOK INTRUSION DETECTION

When the modem is off-hook, an algorithm is implemented in the modem to automatically monitor
the TIP-RING loop current via the LCS register (U63,bits 7:0). Upon detecting an intrusion, the modem alerts the host of the condition via the INT pin. The LCS register has a resolution of 1.1 mAs per bit and returns a zero value if less than the required loop current is present. See 5.1 for details

4.17 OVERCURRENT DETECTION

The SMD24XXL includes an overcurrent detection feature that measures the loop current at a programmable time after the SMD24XXL goes off-hook. This allows the SMD24XXL to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured. See 5.1 for details

4.18 GLOBAL OPERATION

The SMD24XXL chipset contains an integrated silicon direct access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone.

Copyright Delta Design BVBA

4.19 FIRMWARE UPGRADES

The SMD24XXL contains an on-chip program ROM that includes the firmware required for the features listed in this manual. In addition, the SMD24XXL contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows future firmware updates to optimize the characteristics already deployed in the field. See 5.9.1 for complete details.

4.20 AT-COMMANDS

4.20.1 $- Display AT command mode settings.

4.20.2 A-Answer incoming call.

4.20.3 A/ – Re-execute last command.

This is the only command not preceded by “AT” or followed by a <CR>

4.20.4 Dn – Dial

The dial command, followed by 1 or more dial command modifiers, manually dials a phone number.

Syntax

D<string>

Defined Values

<string>	Character string corresponding to the selected option(s).
0-9	DTMF digits 0 to 9.
*	The 'star' digit (tone dialing only).
#	The 'gate' digit (tone dialing only).
A-D	DTMF digits A, B, C, and D.
! or &	Flash hook switch for FHT (U4F) ms (default: 500 ms)
, or <	Pause before continuing for S8 seconds (default:2 seconds)
;	Return to AT command mode
@	Wait for silence.
G	Polarity reversal detect. By placing the “G” character in the dial string (i.e. ATDTG1), the SMD24XXL will monitor the telephone line for polarity reversals. If a busy tone is detected, the SMD24XXL will report “POLARITY REVERSAL” if a polarity reversal was detected or “NO POLARITY REVERSAL” if a polarity reversal was not detected. In each case, the result code is followed by “OK”. If the S7 timeout occurs before a busy tone is detected, the SMD24XXL will report “NO CARRIER”. Polarity reversal monitoring begins after the last digit is dialed and ends when the busy tone is detected or S7 timeout occurs. **Note:** It is not possible to establish a modem connection when using this command.
L	Redial last number.
P	Pulse (rotary) dialing
T	Tone (DTMF) dialing
W	Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1 and X3 do not affect the W command. If the DOP bit (U7A, bit 7) is set, the “ATDTW” command will cause the modem to pause dialing and either report an “OK” if a dialtone is detected or “NO DIALTONE” if a dial tone is not detected.

4.20.5 En –Local DTE Echol

E0	Disable.
E1	Enable (default).

4.20.6 Hn –Hook Switch

H0	Go on-hook (hang up modem)
H1	Go off-hook.

4.20.7 In – Identification and checksum.

I0	Display SMD24XXL revision code.
I1	Display SMD24XXL firmware revision code (numeric).
I3	Display line-side revision code.
I6	Display the modemchip model number. “2493” = Si2493
I7	Diagnostic results 1.
I8	Diagnostic results 2.

4.20.8 Ln – Speaker volume operation

L1	Low speaker volume
L2	Medium speaker volume
L3	High speaker volume

4.20.9 *Mn – Speaker operation*

M0	**Speaker is always off (default)**
M1	Speaker is on while dialing and handshaking; off in data mode.
M2	Speaker is always on.
M3	Speaker is off while dialing, on during handshaking and retraining.

4.20.10 *On – Return to data mode from Command mode operation.*

O0	Return to data mode.
O1	Return to data mode and perform a full retrain (at any speed except 300 bps).
O2	Return to data mode and perform rate renegotiation.

4.20.11 *Qn – Response mode.*

Q0	**Enable result codes(default)**.
Q1	Disable result codes (enable quiet mode).

4.20.12 *R – Initiate V.23 reversal.*

4.20.13 *Sn –S-register operation*

S$	List contents of all S registers.
Sn?	Display contents of S-register n.
Sn=x	Set S-register n to value x (where n and x are decimal values).

4.20.14 *Vn – Result code type*

V0	Numeric result codes.
V1	**Verbal result codes(default)**

4.20.15 *Xn – Call Progress Monitor (CPM)*

This command controls which CPM signals are monitored and reported to the host from the SMD24XXL

X0	Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.
X1	Extended results; disable CPM—Blind dial. CONNECT message includes speed.
X2	Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.
X3	Extended results and detect busy only—Add busy tone detection to X1 mode.
X4	**Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.(default)**
X5	Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.

4.20.16 *Yn – Long space disconnect*

Modem hangs up after 1.5 seconds or more of continuous space while on-line.

Y0	Disable (default)
Y1	Enable

4.20.17 *Z –Reset*

Hard Reset—This command is functionally equivalent to pulsing the RESET pin low.

4.20.18 *:I – Interrupt read*

This command causes the SMD24XXL to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits also are cleared, and the INT pin is deactivated on this read.

4.20.19 *:P – Program RAM write*

Write—This command is used to upload firmware to the SMD24XXL. The format for this command is AT:Paaaa,xxxx,yyyy,.... where aaaa is the first address in hexadecimal and xxxx,yyyy,.... is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is *only* for use with special files. Do not attempt to use this command for any other purpose.
See 5.9.1

4.20.20 *:R – User-Access Register Read*

This command allows the user to read from the user-access registers. The format is “AT:Raa”, where
aa = user-access address in hexadecimal. The “AT:R” command causes all the U- registers to be displayed.

Copyright Delta Design BVBA

4.20.21 :U – User-Access Register Write

This command allows the user to write to the 16-bit user-access registers.
The format is "AT:Uaa,xxxx,yyyy,zzzz,..." where

aa = user-access address in hexadecimal.
xxxx = data in hexadecimal to be written to location aa.
yyyy = data in hexadecimal to be written to location (aa + 1).
zzzz = data in hexadecimal to be written to location (aa + 2).
etc.

4.20.22 +DS- V.42bis Options

Controls V.42bis data compression function.

+DS = A[,B,C,D]

A Direction
- 0 No compression
- 1 Transmit only
- 2 Receive only
- 3 Both directions (default)

B Compression negotiation
- 0 **Do not disconnect if V.42 is not negotiated.(default)**
- 1 Disconnect is V.42 is not negotiated.

C Maximum dictionary size
512

D Maximum string size
6 to 250 (28 default)

4.20.23 +DS44 - V.44 Options (SMD2493L)

Controls V.44 data compression function.

+DS44 = A[,B,C]

A Direction
- 0 No compression
- 1 Transmit only
- 2 Receive only
- 3 Both directions (default)

B Compression negotiation
- 0 **Do not disconnect if V.44 is not negotiated.(default)**
- 1 Disconnect is V.44 is not negotiated.

C Capability
- 0 Stream method

4.20.24 +ES - Enable synchronous assess mode.

+ES = A[,,C]

A Specifies the mode of operation when initiating a modem connection.
- D Disable synchronous assess mode.
- 6 Enable synchronous access mode when connection is completed and data state is entered.

B Specifies fallback mode of operation.
This parameter should not be used.

C Specifies the mode of operation when answer a modem connection.
- D Disable synchronous assess mode.
- 8 Enable synchronous access mode when connection is completed and data state is entered.

4.20.25 +ESA - Synchronous access mode control options.

+ESA = A[,B,C,,E,F,G]

A Specifies action taken if an underrun condition occurs during transparent sub-mode.
- 0 Modem transmits 8-bit SYN sequences on idle.

B Specifies action taken if an underrun condition occurs after a flag during framed submode
- 0 Modem transmits 8-bit HDLC flags on idle.

C Specifies action taken if an underrun or overrun condition occurs after a non-flag during framed sub-mode.
- 0 Modem transmits abort on underrun in middle of frame.
- 1 Modem transmits flag on underrun in middle of frame and notifies host of underrun or overrun.

D Specifies V.34 half duplex operation.
This parameter should not be used.

Copyright Delta Design BVBA

E	Specifies CRC polynomial used while in framed sub-mode. 0 CRC generation checking disable. 1 16-bit CRC generation and checking is performed by the modem.
F	Specifies NRZI encoding and decoding. 0 NRZI encoding and decoding disabled.
G	Specifies SYN. 255 = Fixed at 255 (marks)

4.20.26 +FCLASS=X - Class 1 Mode Enable for V.29 Fast connect

X	Mode
0	Off (default)
1	Enables support for Class 1 mode for use in the V.29 fast connect mode.

4.20.27 +FTM=X - Class 1 Transmit Carrier for V.29 fast connect.

X	Mode
4	Transmit V.21 (980 Hz) tone.
53	Same as &T4, but transmit V.29 7200 bps. Data pattern set by S40 register. AT +FCLASS = 0 must be sent to restore the modem to normal operation after test.
54	Same as &T4, but transmit V.29 9600 bps. Data pattern set by S40 register. AT +FCLASS = 0 must be sent to restore the modem to normal operation after test.
95	V.29 short synchronous.
96	V.29 full synchronous.

4.20.28 +FRM=X - Class 1 Receive Carrier for V.29 fast connect.

X	Mode
4	Transmit V.21 (980 Hz) tone for longer than 100 ms, then send answer tone (2100/2225 Hz) for 200 ms.
95	V.29 short synchronous.
96	V.29 full synchronous.

4.20.29 +GCI=X -Country settings.

Country settings - Automatically configure all registers for a particular country.

X	Country
0	Japan
9	Australia
A	Austria
F	Belgium
16	Brazil
1B	Bulgaria
20	Canada
26	China
27	Columbia
2E	Czech Republic
31	Denmark
35	Ecuador
3C	Finland
3D	France
42	Germany
46	Greece
50	Hong Kong
51	Hungary
53	India
57	Ireland
58	Israel
59	Italy
61	South Korea
69	Luxembourg
6C	Malaysia
73	Mexico
7B	Netherlands
7E	New Zealand
82	Norway
87	Paraguay
89	Philippines
8A	Poland
8B	Portugal
9C	Singapore
9F	South Africa
A0	Spain
A5	Sweden
A6	Switzerland

Copyright Delta Design BVBA

B8	Russia
B4	United Kingdom
B5	United States (default)
FE	Taiwan

Note: U-registers are configured to recommended values. Changes may be made by writing individual registers after sending the AT+GCI command. Several countries use the same configurations as the United Kingdom and the United States.

4.20.30 +GCI? - List current country code setting.

List current country code setting (response is: + GCI:<setting>)

4.20.31 +GCI=? -List all possible country code settings.

4.20.32 +IFC - Specifies the flow control to be implemented.

+IFC=A[,B]

A	Specifies the flow control method used by the host to control data from the modem
- 0	None
- 1	Local XON/OFF flow control. Does not pass XON/XOFF character to the remote modem.
- 2	Hardware flow control (RTS)

B	Specifies the flow control method used by the modem to control data from the host
- 0	None
- 1	Local XON/OFF flow control.
- 2	Hardware flow control (CTS).

4.20.33 +ITF - Transmit flow control threshold.

+ITF=A[,B,C]

A	Threshold above which the modem will generate a flow off signal
<0 to 511> bytes

B	Threshold below which the modem will generate a flow on signal
<0 to 511> bytes

C	Polling interval for <EM><BNUM> indicator
0 to 300 in 10 msec units.

4.20.34 +MR=X - Modulation reporting control

X	Mode
0	Disabled (default)
1	Enabled

If enabled, the intermediate result code is transmitted at the point during connect negotiation.
The format of this result code is as follows:
+MCR: <carrier> e.g. +MCR: V32B
+MRR: <rate> e.g. +MRR: 14400

4.20.35 +MS options - Modulation selection.

+MS=A[,B,C,D,E,F]

A	Prefered modem carrier
- V21	ITU-T V.21
- V22	ITU-T V.22
- V22B	ITU-T V.22bis
- V32	ITU-T V.32
- V32B	ITU-T V.32bis (default SMD2415L)
- V34	ITU-T V.34 (default SMD2434L)
- V90	ITU-T V.90 (default SMD2457L)
- V92	ITU-T V.92 (default SMD2493L)

B	Automatic modulation negotiation
- 0	Disabled
- 1	Enabled

C,D	Min rate/Min rx rate are optional numeric values that specify the lowest value at which the DCE may establish a connection. If unspecified (set to 0), they are determined by the carrier and automode settings.

E,F	Max rate/Max rx rate are optional numeric values which specify the highest value at which the DCE may establish a connection. If unspecified (set to 0), they are deter-mined by the carrier and automode settings.

4.20.36 +PCW=X - Call waiting options

Controls the action to be taken upon detection of call waiting.

X	Mode
0	Toggle RI and collect type II Caller ID if enabled by +VCID.
1	Hang up.
2	Ignore call waiting.(default)

4.20.37 +PIG=X - PCM upstream options

Controls the use of PCM upstream in a V.92 DCE.

X	Mode
0	Enable PCM upstream.(default)
1	Disable PCM upstream.

4.20.38 +PMH=X - Modem-on-hold options

Controls the modem-on-hold procedures.

X	Mode
0	Enables V.92 MOH(default)
1	Disables V.92 MOH.

4.20.39 +PMHF=X - Modem-on-hold hook flash

V.92 MOH hook flash. This command causes the DCE to go on-hook and then return off-hook. If this command is initiated and the modem is not On Hold, Error is returned.

4.20.40 +PMHR=X - Initiate Modem-on-hold

Initiate MOH. Requests the DCE to initiate or to confirm a MOH procedure. Valid only if MOH is enabled.

X	Mode
0	V.92 MOH request denied or not available.
1	MOH with 10 s timeout granted.
2	MOH with 20 s timeout granted.
3	MOH with 30 s timeout granted.
4	MOH with 40 s timeout granted.
5	MOH with 1 min. timeout granted.
6	MOH with 2 min. timeout granted.
7	MOH with 3 min. timeout granted.
8	MOH with 4 min. timeout granted.
9	MOH with 6 min. timeout granted.
10	MOH with 8 min. timeout granted.
11	MOH with 12 min. timeout granted.
12	MOH with 16 min. timeout granted.
13	MOH with indefinite timeout granted.
14	MOH request denied. Future request will also be denied.

4.20.41 +PMHT=X - Initiate Modem-on-hold

Controls access to MOH request and sets the timeout value.

X	Mode
0	Deny V.92 MOH request.
1	Grant MOH with 10 s timeout.
2	Grant MOH with 20 s timeout.
3	Grant MOH with 30 s timeout.
4	Grant MOH with 40 s timeout.
5	Grant MOH with 1 min. timeout.
6	Grant MOH with 2 min. timeout.
7	Grant MOH with 3 min. timeout.
8	Grant MOH with 4 min. timeout.
9	Grant MOH with 6 min. timeout.
10	Grant MOH with 8 min. timeout.
11	Grant MOH with 12 min. timeout.
12	Grant MOH with 16 min. timeout.
13	Grant MOH with indefinite timeout.

4.20.42 +PQC=X - V.92 Phase1 and Phase 2 control

X	Mode
0	Enable Short Phase 1 and Short Phase 2.(default)
1	Enable Short Phase 1.
2	Enable Short Phase 2.
3	Disable Short Phase 1 and Short Phase 2.

Copyright Delta Design BVBA

4.20.43 +PSS=X -startup procedure control

Selection of full or short startup procedures.

X	Mode
0	The DCEs decide to use short startup procedures.(default)
1	Forces the use of short startup procedures on next and subsequent connections.
2	Forces the use of full startup procedures on next and subsequent connections.

4.20.44 +VCDT=X -Caller ID type

X	Mode
0	After ring only (default)
1	Always on
2	UK
3	Japan

4.20.45 +VCID=X -Caller ID Enable

Caller ID Enable.

X	Mode
0	Off(default)
1	On—formatted
2	On—raw data format

4.20.46 +VCIDR? - Type II caller ID information

Type II caller ID information modem will display "+VCDIR:" followed by raw caller ID information including checksum.

4.21 EXTENDED AT& -COMMANDS

4.21.1 &$ – display AT& current settings

4.21.2 &Dn – DTR (ESC) pin options

&D0	ignore
&D1	escapes to command mode from data mode if also enabled by HES U70, bit 15.(default)
&D2	assertion during a modem connection causes the modem to go on-hook and return to command mode.
&D3	assertion causes ATZ command (reset and return OK result code).

4.21.3 &F – Restore factory default settings

4.21.4 &Gn – Line connection rate limit

This command sets an upper limit on the line speed that the SMD24XXL can connect. Note that the &Hn commands may limit the line speed as well (&Gn not used for &H0 or &H1). Not all modulations support rates given by &G. Any improper setting will be ignored. Note that the maximum setting

N	limit (bps max)	
3	1200	
4	2400	default for SMD2404L
5	4800	
6	7200	
7	9600	
8	12000	
9	14400	default for SMD2415L
10	16800	
11	19200	
12	21600	
13	24000	
14	26400	
15	28800	
16	31200	
17	33600	default for SMD2434L/57L/93L

4.21.5 &Hn – PSTN handshake mode

Switched network handshake mode—&Hn commands must be on a separate command line from ATD, ATA, or ATO commands.

N	mode	
0	V.90 with automatic fallback (56 kbps to 300 bps)	(default for SMD2493L/57)
1	V.90 only (56 kbps to 28 kbps)	
2	V.34 with automatic fallback (33.6 kbps to 300 bps)	(default for SMD2434L)
3	V.34 only (33.6 kbps to 2400 bps)	

Copyright Delta Design BVBA

4	ITU-T V.32bis with automatic fallback (14.4 kbps to 300 bps)	(default for SMD2415L)
5	ITU-T V.32bis only (14.4 kbps to 4800 bps)	
6	ITU-T V.22bis only (2400 bps or 1200 bps)	(default for SMD2404L)
7	ITU-T V.22 only (1200 bps)	
8	Bell 212 only (1200 bps)	
9	&H9 Bell 103 only (300 bps)	
10	ITU-T V.21 only (300 bps)	
11	V.23 (1200/75 bps)	

4.21.6 &Pn – Japan pulse dialing

n	mode
0	Configure SM24XX for 10 pulse-per-second pulse dialing. For Japan.
1	Configure SM24XX for 20 pulse-per-second pulse dialing. For Japan.

4.21.7 &Tn – Test mode

n	mode
0	Cancel test mode (Escape to command mode to issue AT&T0). This command will also report the number of bit errors encountered on the previous &T4 test.
1	not used
2	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP only. modem echoes data from TX pin (Register 0 in parallel mode) back to RX pin
3	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP (SMDi24XX), DAA interface section , DAA interface, and analog hybrid circuit. The modem echoes data from TX pin back to RX pin . Phone line termination required. To test only the link operation, the hybrid and AFE codec can be removed from the test loop by setting the DL bit (U62, bit 1).
4	Initiate transmit as originating modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.
5	Initiate transmit as answering modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.
6	Compute checksum for firmware-upgradeable section of program memory. If no firmware upgrade is installed, &T6 returns 0x0408.

4.21.8 &Xn – Automatic determination of telephone line type

n	mode
0	Abort &x1 or &x2 command.
1	Automatic determination of telephone line type. Result code: WXYZn W: 0 = line supports DTMF dialing. 1 = line is pulse dial only. X: 0 = line supports 20 pps dialing. 1 = line supports 10 pps dialing only. Y: 0 = extension network present (PBX). 1 = outside line (PSTN) connected directly. Z: 0 = continuous dialtone. 1 = make-break dialtone. n: 0–9 (number required for outside line if Y = 0).
2	Same as &X1, but Y result (PBX) is not tested.

*4.21.9 *Y2A – Answer tone*

Produce a constant answer tone (ITU-T) and return to command mode. The answer tone continues until the ATH command is received or the S7 timer expires.

4.22 EXTENDED AT% -COMMANDS

4.22.1 %$ – Display AT% command settings

4.22.2 %B – Report blacklist

See also S42 register

4.22.3 %Cn – Data Compression

n	mode
0	Disable V.42bis and MNP5 data compression

Copyright Delta Design BVBA

1 Enable V.42bis in transmit and receive paths. If MNP is selected (\N2), then %C1 enables MNP5 in transmit and receive paths.(default)
2 Enable V.42bis in transmit path only
3 Enable V.42bis in receive path only

4.22.4 %On – Answer mode

n mode
1 SMD24XXL will auto-answer a call in answer mode(default)
2 SMD24XXL will auto-answer a call in originate mode

4.22.5 %Vn – Automatic Line Status detection

After the %V1 and %V2 commands are issued, the modem will automatically check the telephone connection for whether or not a line is present. If a line is present, the modem will automatically check if the line is already in use. Finally, the modem will check line status both before going off-hook and again before dialing. %V1 uses the fixed method and %V2 uses the adaptive method. %V0 (default) disables this feature.

N mode
0 Disable automatic line-in-use detection.(default)
1 Automatic Line Status Detection - Fixed Method.
Description: Before going off-hook with the ATD, ATO, or ATA commands, the modem compares the line voltage (via LVCS) to registers NOLN (U83) and LIUS (U84):

Loop Voltage	Action
0 ≤ LVCS ≤ NOLN	Report “NO LINE” and remain on-hook.
NOLN ≤ LVCS LIUS	Report “LINE IN USE” and remain on-hook.
LIUS ≤ LCVS	Go off-hook and establish a modem connection.

Once the call has begun, the off-hook intrusion algorithm operates normally. In addition, modem will report “NO LINE” if the telephone line is completely disconnected. If the HOI bit (U77, bit 11) is set, “LINE IN USE” is reported upon intrusion.

2 Automatic Line Status Detection - Adaptive Method.
Description: Before going off-hook with the ATD, ATO, or ATA commands, the modem compares the line voltage (via LVCS) to the NLIU (U85) register:

Loop Voltage	Action
0 ≤ LVCS ≤ (0.0625 x NLIU)	Report “NO LINE” and remain on-hook.
(0.0625 x NLIU) < LVCS ≤ (0.85 x NLIU)	Report “LINE IN USE” and remain on-hook.
(0.85 x NLIU) < LCVS	Go off-hook and establish a modem connection.

The NLIU register is updated every 1 ms with the minimum non-zero value of LVCS in the last 30 ms. This allows the SMD24XXL to eliminate errors due to 50/60 Hz interference and also adapt to relatively slow change in the on-hook dc reference value on the telephone line. This algorithm does not allow any non-zero values for NLIU below 0x0007. The host may also initialize NLIU prior to issuing the %V2 command. Once the call has begun, the off-hook intrusion algorithm (described in "Off-Hook Intrusion Detection" on page 18) operates normally. In addition, modem will report “NO LINE” if the telephone line is completely disconnected.
If the HOI (U77, bit 11) bit is set, “LINE IN USE” is reported upon intrusion.

4.23 EXTENDED AT\ -COMMANDS

4.23.1 \$ – Display AT\ command settings

4.23.2 \Bn – Character length

Character length will be automatically set in autobaud mode

N mode
0 6N1—six data bits, no parity, one stop bit, one start bit, eight bits total (\N0 only)1
1 7N1—seven data bits, no parity, one stop bit, one start bit, nine bits total (\N0 only)1
2 7P1—seven data bits, parity optioned by \P, one stop bit, one start bit, 10 bits total
3 8N1—eight data bits, no parity, one stop bit, one start bit, 10 bits total (default)
5 8P1—eight data bits, parity optioned by \P, one stop bit, one start bit, 11 bits total (\N0 only)
6 8X1—eight data bits, one escape bit, one stop bit, one start bit, 11 bits total (enables ninth-bit escape mode)

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T9 if a resistor is installed in position R23; otherwise, the default is \T16. (See "Autobaud" 5.8.)

4.23.3 \Nn – Asynchrounous protocol

n mode
0 Wire mode (no error correction, no compression)

1 MNP reliable mode. The modem attempts to connect with the MNP protocol. If unsuccessful, the call is dropped.
3 V.42 auto-reliable—The modem attempts to connect with the V.42 protocol. If unsuccessful, the MNP protocol is attempted. If unsuccessful, wire mode is attempted (default).
4 V.42 (LAPM) reliable mode (or drop call)—Same as \N3 except that the modem drops the call instead of connecting in MNP or wire mode.
5 V.42 and MNP reliable mode—The modem attempts to connect with V.42. If unsuccessful, MNP is attempted. If MNP us unsuccessful, the call is dropped.

4.23.4 \Pn – Parity type

Parity type will be automatically set in autobaud mode

N	mode
0	even (default)
1	space
2	Odd
3	Mark

4.23.5 \Qn – Modem-to-DTE flow control

n	mode
0	Disable all flow control—This may only be used if the DTE speed and the VF speed are guaranteed to match throughout the call.
2	Use CTS only (default)
3	Use RTS/CTS
4	Use XON/XOFF flow control for modem-to-DTE interface. Does not enable modem-to-modem flow control.

4.23.6 \Tn – DTE rate

Change DTE rate. When the modem is configured in autobaud mode (default), \T0 through \T15 will lock the new baud rate and disable autobaud. When the modem is not in autobaud mode the result code “OK” is sent at the old DTE rate. Subsequent commands must be sent at the new rate.

N	rate (bps)
0	300
1	600
2	1200
3	2400
4	4800
5	7200
6	9600
7	12000
8	14400
9	19200
10	38400
11	57600
12	115200
13	230400
14	245760
15	307200
16	Autobaud (default)
17	Autobaud off, look at current baud rate

1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T9 if a 10K resistor is installed in position R23 ; otherwise, the default is \T16. (See "Autobaud" 5.8.)

4.23.7 \Un – RI , DCD

causes a low pulse (25 ms) on RI and DCD. INT to be the inverse of DTR (ESC). RTS to be inverse of CTS.

4.23.8 \Vn – Connect message type

n	type
0	Report connect message and protocol message (default)
2	Report connect message only (exclude protocol message)
4	Report connect and protocol message with both upstream and downstream connect rates.

4.24 RESULT CODES

Numeric	Meaning	Verbal response	X0	X1	X2	X3	X4	X5
0	Command was successful	OK	X	X	X	X	X	X
1	Link established at 300bps or higher	CONNECT	X	X	X	X	X	X

2	Incoming ring detected	RING	X	X	X	X	X	X
3	Link dropped	NO CARRIER	X	X	X	X	X	X
4	Command failed	ERROR	X	X	X	X	X	X
5	Link established at 1200	CONNECT 1200		X	X	X	X	X
6	Dial tone not present	NO DIALTONE			X	X	X	X
7	Line busy	BUSY				X	X	X
8	Remote not answering	NO ANSWER	X	X	X	X	X	X
9	Ringback detected	RINGING						X
10	Link established at 2400			X	X	X	X	X
11	Link established at 4800			X	X	X	X	X
12	Link established at 9600			X	X	X	X	X
14	Link established at 19200			X	X	X	X	X
15	Link established at 7200			X	X	X	X	X
16	Link established at 12000			X	X	X	X	X
17	Link established at 14400			X	X	X	X	X
18	Link established at 16800			X	X	X	X	X
19	Link established at 21600			X	X	X	X	X
20	Link established at 24000			X	X	X	X	X
21	Link established at 26400			X	X	X	X	X
22	Link established at 28800			X	X	X	X	X
23	Link established at 31200			X	X	X	X	X
24	Link established at 33600			X	X	X	X	X
30	Caller ID mark detected	CIDM	X	X	X	X	X	X
31	Hookswitch flash detected	FLASH	X	X	X	X	X	X
32	UK CID State Tone Alert Signal detected	STAS	X	X	X	X	X	X
33	Overcurrent detection	X (note 1)	X	X	X	X	X	X
40	Blacklist is full	BLACKLIST FULL (enabled via S42 register)	X	X	X	X	X	X
41	Attempted number is blacklisted	BLACKLISTED (enabled via S42 register)	X	X	X	X	X	X
42	No phone line present	NO LINE (enabled via %Vn commands)	X	X	X	X	X	X
43	Telephone line is in use	LINE IN USE (enabled via %Vn commands)	X	X	X	X	X	X
44	A polarity reversal was detected	POLARITY REVERSAL (enabled via G modifier)	X	X	X	X	X	X
45	A polarity reversal was NOT detected	NO POLARITY REVERSAL (enabled via G modifier)		X	X	X	X	X
52	Link established at 56000	CONNECT 56000		X	X	X	X	X
60	Link established at 32000	CONNECT 32000		X	X	X	X	X
61	Link established at 48000	CONNECT 48000		X	X	X	X	X
63	Link established at 28000	CONNECT 28000		X	X	X	X	X
64	Link established at 29333	CONNECT 29333		X	X	X	X	X
65	Link established at 30666	CONNECT 30666		X	X	X	X	X
66	Link established at 33333	CONNECT 33333		X	X	X	X	X
67	Link established at 34666	CONNECT 34666		X	X	X	X	X
68	Link established at 36000	CONNECT 36000		X	X	X	X	X
69	Link established at 37333	CONNECT 37333		X	X	X	X	X
70	No protocol	PROTOCOL: NONE	Set with \V0 command					
75	Link established at 75	CONNECT 75		X	X	X	X	X
77	V.42 protocol	PROTOCOL: V42	Set with \V0 command					
79	V.42bis protocol	PROTOCOL: V42bis	Set with \V0 command					
80	MNP2 protocol	PROTOCOL: ALTERNATE,+CLASS 2	Set with \V command					
81	MNP3 protocol	PROTOCOL: ALTERNATE,+CLASS 3	Set with \V command					
82	MNP4 protocol	PROTOCOL: ALTERNATE,+CLASS 4	Set with \V command					
83	MNP5 protocol	PROTOCOL: ALTERNATE,+CLASS 5		X	X	X	X	X
90	Link established at 38666	CONNECT 38666		X	X	X	X	X
91	Link established at 40000	CONNECT 40000		X	X	X	X	X
92	Link established at 41333	CONNECT 41333		X	X	X	X	X
93	Link established at 42666	CONNECT 42666		X	X	X	X	X
94	Link established at 44000	CONNECT 44000		X	X	X	X	X
95	Link established at 45333	CONNECT 45333		X	X	X	X	X
96	Link established at 46666	CONNECT 46666		X	X	X	X	X
97	Link established at 49333	CONNECT 49333		X	X	X	X	X

Copyright Delta Design BVBA

98	Link established at 50666	CONNECT 50666		X	X	X	X	X
99	Link established at 52000	CONNECT 52000		X	X	X	X	X
100	Link established at 53333	CONNECT 53333		X	X	X	X	X
101	Link established at 54666	CONNECT 54666		X	X	X	X	X
102	DTMF dial attempted on a pulse dial only line	UN-OBTAINABLE NUMBER	X	X	X	X	X	X

Note 1: X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.

4.25 S-REGISTERS

The S command allows reading (Sn?) or writing (Sn = x) the S-registers. The S-registers store values for functions that typically are rarely changed, such as timers or counters, and the ASCII values of control characters, such as carriage return. The table blow summarizes the S-register set.

Definition				
S-register (Decimal)	**Function**	**Default (decimal)**	**Range**	**Units**
0	Automatic answer – Number of rings the modem must detect before answering a call. O disables auto answer	0	0-255	Rings
1	Ring Counter	0	0-255	Rings
2	ESC code character	43(+)	0-255	ASCII
3	Carriage return character	13(CR)	0-255	ASCII
4	Linefeed character	10(LF)	0-255	ASCII
5	Backspace character	08(BS)	0-255	ASCII
6	Dial tone wait timer – Number of seconds the modem waits before blind dialing. Only applicable if blind dialing is enabled(X0,X1,X3)	02	0-255	seconds
7	Carrier Wait timer – Number waits for carrier before timing out. This register also sets the number of seconds the modem waits for ring-backwhen originating a call before hanging up. This register also sets the number of seconds the answertone will continue while using the AT *Y2A command.	80	0-255	seconds
8	Dial pause timer for , and < dial command modifiers.	02	0-255	seconds
9	Carrier presence timer – Time after a loss of carrier that a carrier must be detected before reactivating DCD. S9 is referred to as "carrier loss debounce time."	06	1-255	0.1 second
10	Carrier loss timer – Time the carrier be lost before the SMD24XXL disconnects. Setting 255 disables disconnect entirely. If S10 is less than S9, even a momentary loss of carrier causes a disconnect.	14	1-255	0.1 second
12	Escape code guard timer—Minimum guard time required before and after "+++" for the SMD24XXL to recognize a valid escape sequence.	50	1-255	0.02 second
14	Wait for dial tone delay value (in relation to the W dial modifier). Starts when "W" is executed in the dial string.	12	0-255	seconds
24	Sleep Inactivity Time—Sets the time that the modem operates in normal power mode with no activity on the serial port, parallel port, or telephone line before enter-ing low-power sleep mode. This feature is disabled if the timer is set to 0.	0	0-255	seconds
30	Disconnect Activity Timer—Sets the length of time that the modem stays online before disconnecting with no activity on the serial port, parallel port, or telephone line (Ring, hookswitch flash, or caller ID). This feature is disabled if set to 0.	0	0-255	minutes
38	Hang Up Delay Time—Maximum delay between receipt of ATH0 command and hang up. If time out occurs before all data can be sent, the NO CARRIER (3) result code is sent (operates in V.42 mode only). "OK" response is sent if all data is transmitted before timeout. S38 = 255 disables timeout and modem disconnects only if data is successfully sent or carrier is lost.	20	0-255	seconds
40	Data Pattern—Data pattern generated during &T4 and &T5 transmit tests. 0 – All spaces (0s) 1 – All marks (1s) 2 – Random data	0	0-2	
41	V.34 symbol rate - Symbol rate for V.34 when using the &T4 and &T5 commands. **0 – 2400 symbols/second** 1 – 2743 symbols/second 2 – 2800 symbols/second 3 – 3000 symbols/second 4 – 3200 symbols/second	0	0-5	

Copyright Delta Design BVBA

	5 – 3429 symbols/second A valid combination of symbol rate (S41) and data rate (&G) must be selected. **Symbol Rate Allowable Data Rates** 2400 2400 – 21600 2743 4800 – 26400 2800 4800 – 26400 3000 4800 – 28800 3200 4800 – 31200 3429 4800 – 33600			
42	Blacklisting—The SMD24XXL will not dial the same number more than two times in three minutes. An attempt to dial a third time within three minutes will result in a “BLACKLISTED” result code. If the blacklist memory is full, any dial to a new number will result in a “BLACK-LIST FULL” result code. Numbers are added to the blacklist only if the modem connection fails. The %B command will list the numbers on the blacklists. 0 = disabled 1 = enabled	0	0-1	
43	Dial attempts to blacklist When blacklisting is enabled with S42, this value controls the number of dial attempts that will result in a number being blacklisted.	4	0-4	-
44	Blacklist Timer Period during which blacklisting is active	180	0-255	seconds
50	Minimum on-hook time—Modem will remain on-hook for S50 seconds. Any attempt to go off-hook will be delayed until this timer expires.	3	0-255	seconds
51	Number to start checking for an outside line on a PBX.	1	0-9	-

4.26 USER-ACCESS REGISTERS (U-REGISTERS)

U-Registers (user-access registers) are 16-bit registers directly written by the AT:Uaa command and read by the AT:R (read all U-Registers) or AT:Raa (read U-Register aa) commands.
The U-Register number is the last two digits of the register’s hexadecimal address. All values associated with the U-Registers, the address, and the value written to or read from the register are hexadecimal. Some U-Registers are reserved and not available to the user. Therefore, there are gaps in the available U-Register address sequence. Additionally, some bits within available U-Registers are reserved. Any attempt to write to a non-listed U-Register or to write a reserved bit to a value other than 0 b causes unpredictable modem operation. There are two types of U-Registers. The first represents a single 16-bit term, such as a filter coefficient, threshold, delay, or other quantity. These registers can be read from or written to as a single 16-bit value. The second type of U-Register is bit-mapped. Bit-mapped registers are written and/or read in hexadecimal, but each bit or combination of bits in the register represents an independent value or status information. These individual bits are used to enable or disable features and indicate states. Groups of bits in a bit-mapped register can be used to represent a value. Bits in these registers can be read/write, read only, or reserved, or they may be required to be set as a 1 or 0. Most reserved bits return a 0 when read. Pay particular attention when writing to bit-mapped registers to ensure no reserved bits are overwritten. All U-Registers revert to their default setting after a reset. The U-Registers can be broken into three groups: Call Progress (U0–U33, U49–U4C), Dialing (U37–U48), and Line Interface and Extended Functions (U4D–UA9).

Register	Name	Description	Default
U00	DT1A0	DT1 registers set the coefficients for stage 1 of the Dial Tone Detect filter. Default is for FCC countries.	0x0800
U01	DT1B1		0x0000
U02	DT1B2		0x0000
U03	DT1A2		0x0000
U04	DT1A1		0x0000
U05	DT2A0	Dial tone detect filters stage 2 biquad coefficients.	0x00A0
U06	DT2B1		0x6EF1
U07	DT2B2		0xC4F4
U08	DT2A2		0xC000
U09	DT2A1		0x0000
U0A	DT3A0	Dial tone detect filters stage 3 biquad coefficients.	0x00A0
U0B	DT3B1		0x78B0
U0C	DT3B2		0xC305
U0D	DT3A2		0x4000
U0E	DT3A1		0xB50A
U0F	DT4A0	Dial tone detect filters stage 4 biquad coefficients.	0x0400
U10	DT4B1		0x70D2
U11	DT4B2		0xC830
U12	DT4A2		0x4000
U13	DT4A1		0x80E2
U14	DTK	Dial tone detect filter output scaler.	0x0009
U15	DTON	Dial tone detect ON threshold.	0x00A0
U16	DTOF	Dial tone detect OFF threshold.	0x0070

U17	BT1A0	BT1 registers set the coefficients for stage 1 of the Busy Tone Detect filter.	0x0800
U18	BT1B1		0x0000
U19	BT1B2		0x0000
U1A	BT1A2		0x0000
U1B	BT1A1		0x0000
U1C	BT2A0	Busy tone detect filter stage 2 biquad coefficients.	0x00A0
U1D	BT2B1		0x6EF1
U1E	BT2B2		0xC4F4
U1F	BT2A2		0xC000
U20	BT2A1		0x0000
U21	BT3A0	Busy tone detect filter stage 3 biquad coefficients.	0x00A0
U22	BT3B1		0x78B0
U23	BT3B2		0xC305
U24	BT3A2		0x4000
U25	BT3A1		0xB50A
U26	BT4A0	Busy tone detect filter stage 4 biquad coefficients.	0x0400
U27	BT4B1		0x70D2
U28	BT4B2		0xC830
U29	BT4A2		0x4000
U2A	BT4A1		0x80E2
U2B	BTK	Busy tone detect filter output scaler.	0x0009
U2C	BTON	Busy tone detect ON threshold.	0x00A0
U2D	BTOF	Busy tone detect OFF threshold.	0x0070
U2E	BMTT	Busy cadence minimum total time in seconds multiplied by 7200.	0x0870
U2F	BDLT	Busy cadence delta in seconds multiplied by 7200.	0x25F8
U30	BMOT	Busy cadence minimum on time in seconds multiplied by 7200.	0x0438
U31	RMTT	Ringback cadence minimum total time in seconds multiplied by 7200.	0x4650
U32	RDLT	Ringback cadence delta in seconds multiplied by 7200.	0xEF10
U33	RMOT	Ringback cadence minimum on time in seconds multiplied by 7200.	0x1200
U34	DTWD	Window to look for dialtone in seconds multiplied by 1000.	0x1B58
U35	DMOT	Minimum dialtone on time in seconds multiplied by 7200.	0x2D00
U37	PD0	Number of pulses to dial 0.	0x000A
U38	PD1	Number of pulses to dial 1.	0x0001
U39	PD2	Number of pulses to dial 2.	0x0002
U3A	PD3	Number of pulses to dial 3.	0x0003
U3B	PD4	Number of pulses to dial 4.	0x0004
U3C	PD5	Number of pulses to dial 5.	0x0005
U3D	PD6	Number of pulses to dial 6.	0x0006
U3E	PD7	Number of pulses to dial 7.	0x0007
U3F	PD8	Number of pulses to dial 8.	0x0008
U40	PD9	Number of pulses to dial 9.	0x0009
U42	PDBT	Pulse dial break time (ms units).	0x003D
U43	PDMT	Pulse dial make time (ms units).	0x0027
U45	PDIT	Pulse dial interdigit time (ms units).	0x0320
U46	DTPL	DTMF power level—16-bit format is 0x0(H)(L)0 where H is the (–)dBm level of the high-frequency DTMF tone and L is the (–)dBm level of the low-frequency DTMF tone. Note that twist may be specified here.	0x09B0
U47	DTNT	DTMF on time (ms units).	0x0064
U48	DTFT	DTMF off time (ms units).	0x0064
U49	RGFH	Ring frequency high—Maximum frequency ring to be considered a valid ring. RGFH = 2400/(maximum ring frequency).	0x0022
U4A	RGFD	Ring delta	0x007A
U4B	RGMN	Ring cadence minimum ON time in seconds multiplied by 2400.	0x0258
U4C	RGNX	Ring cadence maximum total time in seconds multiplied by 2400.	0x6720
U4D	MOD1	This is a bit-mapped register.	0x0000
U4E	PRDD	Pre-dial delay-time after ATD command that modem waits to dial (ms units). The modem stays on-hook during this time.	0x0000
U4F	FHT	Flash Hook Time. Time corresponding with "!" or "&" dial modifier that the SMD24XXL goes on-hook during a flash hook (ms units).	0x01F4
U50	LCDN	Loop current debounce on time (ms units).	0x015E
U51	LCDF	Loop current debounce off time (ms units).	0x00C8
U52	XMTL	Transmit level (1 dB units)—Sets the modem data pump transmitter level. Default level of 0 corresponds to –9.85 dBm. Transmit level = –(9.85 + XMTL) dBm. Range = –9.85 to –48.	0x0000
U53	MOD2	This is a bit-mapped register.	0x0000
U62	DAAC1	This is a bit-mapped register.	0x0804
U63	DAAC3	This is a bit-mapped register.	
U65	DAAC4	This is a bit-mapped register.	0x00E0
U66	DAAC5	This is a bit-mapped register.	0x0040

Copyright Delta Design BVBA

U67	ITC1	This is a bit-mapped register.	0x0008
U68	ITC2	This is a bit-mapped register.	0x0000
U6A	ITC4	This is a bit-mapped register.	N/A
U6C	LVS	This is a bit-mapped register.	0x0000
U6E	CK1	This is a bit-mapped register.	0x1F20
U67	PTMR	This is a bit-mapped register.	0x00FF
U70	IO0	This is a bit-mapped register.	0x2700
U71	IO1	This is a bit-mapped register.	0x0000
U76	GEN1	This is a bit-mapped register.	0x3240
U77	GEN2	This is a bit-mapped register.	0x401E
U78	GEN3	This is a bit-mapped register.	0x0000
U79	GEN4	This is a bit-mapped register.	0x0000
U7A	GENA	This is a bit-mapped register.	0x0000
U83	NOLN	No-Line threshold. If %V1 is set, NOLN sets the threshold for determination of line present vs. line not present.	0x0001
U84	LIUS	Line-in-use threshold. If %V1 is set, LIUS sets the threshold for determination of line in use vs. line not in use.	0x0007
U85	NLIU	Line-in-use/No line threshold. If %V2 is set, NLIU sets the threshold reference for the adaptive algorithm (see %V2).	0x0000
U86	V9AGG	V.90 rate adjustment for Japan 1333 BPS units	0x0000
U87	SAM	This is a bit-mapped register	0x0000
U9F	SASF	SAS frequency detection.	0x0000
UA0	SC0	SAS cadence 0. Sets the duration of the first SAS tone (ms).	0x01E0
UA1	SC1	SAS cadence 1. Sets the duration of the first SAS silence (ms).	0x0000
UA2	SC2	SAS cadence 2. Sets the duration of the second SAS tone (ms).	0x0000
UA3	SC3	SAS cadence 3. Sets the duration of the second SAS silence (ms).	0x0000
UA4	SC4	SAS cadence 4. Sets the duration of the third SAS tone (ms).	0x0000
UA5	SC5	SAS cadence 5. Sets the duration of the third SAS silence (ms).	0x0000
UA6	SC6	SAS cadence 6. Sets the duration of the fourth SAS tone (ms).	0x0000
UA7	SC7	SAS cadence 7. Sets the duration of the fourth SAS silence (ms).	0x0000
UA8	SC8	SAS cadence 8. Sets the duration of the fifth SAS tone (ms).	0x0000
UA9	SC9	SAS cadence 9. Sets the duration of the fifth SAS silence (ms).	0x0000
UAA	V29MODE	This is a bit mapped register.	0x0000

Copyright Delta Design BVBA

Bit-Mapped U-Register summary

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U4D	MOD1		TOCT		NHFP	NHFD	CLPD		FTP	SPDM		GT18	GT55	CTE			
U53	MOD2	REV															
U62	DAAC1								OHS2						FOH	DL	
U63	DAAC3									ACT[3:0]							
U65	DAAC4		PWMG	PDN									PDL				
U66	DAAC5										FDT						
U67	ITC1			MINI[1:0]				ILIM		OFF	OHS			DCV[1:0]		RZ	RT
U68	ITC2														BTE	ROV	BTD
U6A	ITC4														OVL		
U6C	LVS	LVS[7:0]															
U6E	CK1					R1[4:0]											
U6F	PTME									PTMR[7:0]							
U70	IO0	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
U71	IO1												COMP				PRT
U76	GEN1	OHSR[6:0]							FACL	DCL[2:0]			ACL[4:0]				
U77	GEN2	IST[3:0]				HOI		AOC	OHT[8:0]								
U78	GEN3	IB[1:0]								IS[7:0]							
U79	GEN4												LVCS[4:0]				
U7A	GENA									DOP	ADD				V22HD	HDLC	FAST
U7C	GENC												RIGPO				RIG-POEN
U7D	GEND															ATZD	FDP
U87	SAM						MINT	SERM	FSMS	XMTT							
UAA	V29MODE															V29ENA	

Copyright Delta Design BVBA

4.27 BIT_MAPPED U-REGISTER DETAIL

U-Registers are identified with the letter “U” followed by the last two digits of the register’s hexadecimal address. Values written to or read from these registers are in hexadecimal format. Country-specific register values are presented in "Country Dependent Setup" . All default settings are chosen to meet FCC requirements.

4.27.1 U00-U16 Dial Tone Detect filter registers

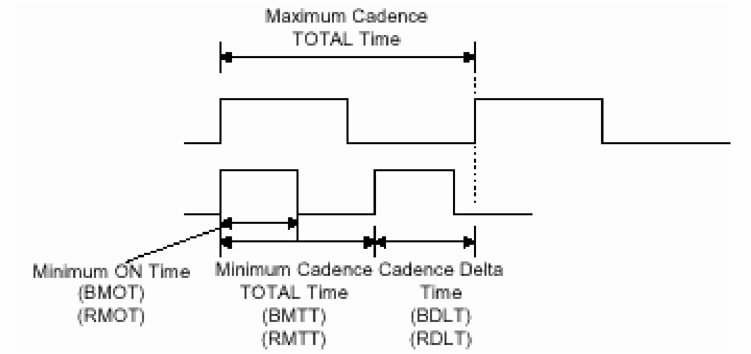
U00–U13 set the biquad filter coefficients for stages 1–4of the Dial Tone detect filter, and U14, U15, and U16 set the Dial Tone detect output scaler, on threshold and off threshold, respectively. The thresholds are empirically found scalars and have no units. These coefficients are programmed as 16-bit 2’s complement values. All A0 values are in 3.12 format where 1.0 = 0x1000. All other coefficients are in 1.14 format where 1.0 = 0xC000.
Default settings meet FCC requirements. Additionally, register U34 sets the time window in which dial tone can be detected. Register U35 sets the minimum time within the U34 window that the dial tone must be present for a valid detection. See "U34–U35 (Dial Tone Timing)" for more information.

Register	Name	Description	Default
U00	DT1A0	DT1 registers set the coefficients for stage 1 of the Dial Tone Detect filter. Default is for FCC countries.	0x0800
U01	DT1B1		0x0000
U02	DT1B2		0x0000
U03	DT1A2		0x0000
U04	DT1A1		0x0000
U05	DT2A0	Dial tone detect filters stage 2 biquad coefficients.	0x00A0
U06	DT2B1		0x6EF1
U07	DT2B2		0xC4F4
U08	DT2A2		0xC000
U09	DT2A1		0x0000
U0A	DT3A0	Dial tone detect filters stage 3 biquad coefficients.	0x00A0
U0B	DT3B1		0x78B0
U0C	DT3B2		0xC305
U0D	DT3A2		0x4000
U0E	DT3A1		0xB50A
U0F	DT4A0	Dial tone detect filters stage 4 biquad coefficients.	0x0400
U10	DT4B1		0x70D2
U11	DT4B2		0xC830
U12	DT4A2		0x4000
U13	DT4A1		0x80E2
U14	DTK	Dial tone detect filter output scaler.	0x0009
U15	DTON	Dial tone detect ON threshold.	0x00A0
U16	DTOF	Dial tone detect OFF threshold.	0x0070

4.27.2 U17-U30 Busy Tone Detect filter registers

U17–U2A set the biquad filter coefficients for stages 1–4 of the Busy Tone detect filter, and U2B, U2C, and U2D set the Busy Tone detect output scalar, on threshold and off threshold, respectively. The thresholds are empirically found scalars and have no units. These coefficients are programmed as 16-bit 2’s complement values. All A0 values are in 3.12 format where 1.0 = 0x1000. All other coefficients are in 1.14 format where 1.0 = 0xC000. Default values meet FCC requirements.
U2E, U2F, and U30 set the busy cadence minimum total time (BMTT), busy cadence delta time (BDLT), and busy cadence minimum on time (BMOT), respectively. Settings for busy cadences are specified as a range for ON time (minimum ON and maximum ON) and a range for OFF time (minimum OFF and maximum OFF). The three values represented by BMTT, BDLT, and BMOT fully specify these ranges. BMTT, minimum total time, is equal to the minimum ON time plus the minimum OFF time. BDLT (allowable delta) is equal to the maximum total time (maximum ON time plus the maximum OFF time) minus the minimum total time (BMTT). BMOT is the minimum ON time. The values stored in the registers are the hexadecimal representation of the times in seconds multiplied by 7200. Default values meet FCC requirements.

Copyright Delta Design BVBA



Example: The United States specifies a busy tone with on time from 450 to 550 ms and off time from 450 to 550 ms. Thus, minimum ON time equals 0.450 s, maximum ON time equals 0.550 s, minimum OFF time equals 0.450 sec, and maximum OFF time equals 0.550 sec. Busy Cadence Minimum Total Time = 0.450 s + 0.450 s = 0.900 s. Therefore, BMTT = (0.900)(7200)d = 0x1950. Maximum total time = 0.550 s + 0.550 s = 1100 ms, so BDLT = (1.10– 0.900)(7200)d = 0x05A0, and BMOT = (0.450)(7200)d = 0x0CA8. The hexadecimal values are stored in the appropriate registers using the AT:Uaa command where aa is the U-Register number (hexadecimal address). Detection parameters can be wider than the minimum specifications. This is often done in the modem defaults and other suggested settings so that one set of parameters can cover a large number of different country requirements.

Register	Name	Description	Default
U17	BT1A0	BT1 registers set the coefficients for stage 1 of the Busy Tone Detect filter.	0x0800
U18	BT1B1		0x0000
U19	BT1B2		0x0000
U1A	BT1A2		0x0000
U1B	BT1A1		0x0000
U1C	BT2A0	Busy tone detect filter stage 2 biquad coefficients.	0x00A0
U1D	BT2B1		0x6EF1
U1E	BT2B2		0xC4F4
U1F	BT2A2		0xC000
U20	BT2A1		0x0000
U21	BT3A0	Busy tone detect filter stage 3 biquad coefficients.	0x00A0
U22	BT3B1		0x78B0
U23	BT3B2		0xC305
U24	BT3A2		0x4000
U25	BT3A1		0xB50A
U26	BT4A0	Busy tone detect filter stage 4 biquad coefficients.	0x0400
U27	BT4B1		0x70D2
U28	BT4B2		0xC830
U29	BT4A2		0x4000
U2A	BT4A1		0x80E2
U2B	BTK	Busy tone detect filter output scaler.	0x0009
U2C	BTON	Busy tone detect ON threshold.	0x00A0
U2D	BTOF	Busy tone detect OFF threshold.	0x0070
U2E	BMTT	Busy cadence minimum total time in seconds multiplied by 7200.	0x0870
U2F	BDLT	Busy cadence delta in seconds multiplied by 7200.	0x25F8
U30	BMOT	Busy cadence minimum on time in seconds multiplied by 7200.	0x0438

4.27.3 U31-U33 Ringback Cadence Registers

U31, U32, and U33 set the ringback cadence minimum total time (RMTT), ringback cadence delta time (RDLT), and ringback cadence minimum on time (RMOT). Country-specific settings for ringback cadences are specified as a range for ON time (minimum ON and maximum ON) and a range for OFF time (minimum OFF and maximum OFF). The three values represented by RMTT, RDLT, and RMOT fully specify these ranges. RMTT, minimum total time, is equal to the minimum ON time plus the minimum OFF time. RDLT (allowable delta) is equal to the maximum total time (maximum ON time plus the maximum OFF time) minus the minimum total time (RMTT). RMOT is the minimum ON time. The values stored in the registers are the hexadecimal representation of the times in seconds multiplied by 7200. Default values meet FCC requirements.

Register	Name	Description	Default
U31	RMTT	Ringback cadence minimum total time in seconds multiplied by 7200.	0x4650
U32	RDLT	Ringback cadence delta in seconds multiplied by 7200.	0xEF10
U33	RMOT	Ringback cadence minimum on time in seconds multiplied by 7200.	0x1200

4.27.4 U34-U35 Dial tone timing

U34 determines the period of time the modem attempts to detect a dial tone. U35 sets the time within this window the dial tone must be present in order to return a valid dial tone detection. The value stored in U35 is the hexadecimal representation of the

Copyright Delta Design BVBA

time in seconds multiplied by 7200. The value in U34 is the hexadecimal representation of the time in seconds multiplied by 1000. The time window represented in U34 must be larger than the dial tone present time represented in register U35.

Register	Name	Description	Default
U34	DTWD	Window to look for dialtone in seconds multiplied by 1000.	0x1B58
U35	DMOT	Minimum dialtone on time in seconds multiplied by 7200.	0x2D00

4.27.5 U37-U45 Pulse Dial Registers

Registers U37–U40 set the number of pulses to dial digits 0 through 9, respectively. The values are entered in hexadecimal format with digit 0 having a default setting of 0x000A (10 decimal) pulses, digit 1 having a default setting of one pulse, digit 2 having a default setting of two pulses, etc. This pulse arrangement is used throughout most of the world. There are, however, two exceptions—New Zealand and Sweden. New Zealand requires 10 pulses for 0, nine pulses for 1, eight pulses for 2, etc. Sweden, on the other hand, requires one pulse for 0, two pulses for 1, etc. Complete information is provided in "Country Dependent Setup" .

U42, U43, and U45 set the pulse dial break-time (PDBT), make-time (PDMT), and inter-digit delay time (PDIT), respectively. The values are entered in hexadecimal format and represent ms units. The default values meet FCC requirements. The default dialing speed is 10 pps. See "Country Dependent Setup" for Japanese 20 pps dialing configuration.

Register	Name	Description	Default
U37	PD0	Number of pulses to dial 0.	0x000A
U38	PD1	Number of pulses to dial 1.	0x0001
U39	PD2	Number of pulses to dial 2.	0x0002
U3A	PD3	Number of pulses to dial 3.	0x0003
U3B	PD4	Number of pulses to dial 4.	0x0004
U3C	PD5	Number of pulses to dial 5.	0x0005
U3D	PD6	Number of pulses to dial 6.	0x0006
U3E	PD7	Number of pulses to dial 7.	0x0007
U3F	PD8	Number of pulses to dial 8.	0x0008
U40	PD9	Number of pulses to dial 9.	0x0009
U42	PDBT	Pulse dial break time (ms units).	0x003D
U43	PDMT	Pulse dial make time (ms units).	0x0027
U45	PDIT	Pulse dial interdigit time (ms units).	0x0320

4.27.6 U46-48 DTMF dial registers

U46–U48 set the DTMF power level, DTMF on time, and DTMF off time, respectively. The DTMF power level set in register U46 is a 16-bit hexadecimal value with the format 0x0(H)(L)0. Where H is a hexadecimal number (0–F) for the dBm level of the high-frequency DTMF tone, and L is a hexadecimal number (0–F) for the dBm level of the low-frequency DTMF tone. The difference between the level of the high-frequency tone and the low-frequency tone is called “twist” and can be set with the choice of the H and L values in –1 dBm steps. The DTMF output level is 0 dBm for each tone if U46 = 0x0000 and –15 dBm if U46 = 0x0FF0. The default power level is –9 dBm for the high tone and –11 dBm for the low tone.

U47 and U48 set the DTMF on time (DTNT) and DTMF off time (DTFT) respectively as a hexadecimal value with ms units. The default value for both U47 and U48 is 100 ms, and the range of values is 0–1000 ms.

Register	Name	Description	Default
U46	DTPL	DTMF power level—16-bit format is 0x0(H)(L)0 where H is the (–)dBm level of the high-frequency DTMF tone and L is the (–)dBm level of the low-frequency DTMF tone. Note that twist may be specified here.	0x09B0
U47	DTNT	DTMF on time (ms units).	0x0064
U48	DTFT	DTMF off time (ms units).	0x0064

4.27.7 U49-U4C Ring Detect Registers

U49, U4A, U4B, and U4C set a representation of the maximum ring frequency, the difference between the highest and lowest valid ring frequency, minimum ring on time, and maximum ring cadence time (time on + time off), respectively. U49 is set as the hexadecimal equivalent of 2400 divided by the highest valid ring frequency in Hz. U4A is set as the hexadecimal equivalent of 2400 divided by the minimum valid ring frequency in Hertz minus 2400 divided by the maximum valid ring frequency in Hertz. U4B and U4C are set as the hexadecimal equivalents of the times in seconds multiplied by 2400. The default high ring frequency, RGFH (U49), is 70.6 Hz. The default ring cadence minimum on time, RGMN, is 250 ms. The default ring cadence maximum total time is 11 seconds.

Register	Name	Description	Default
U49	RGFH	Ring frequency high—Maximum frequency ring to be considered a valid ring. RGFH = 2400/(maximum ring frequency).	0x0022
U4A	RGFD	Ring delta	0x007A
U4B	RGMN	Ring cadence minimum ON time in seconds multiplied by 2400.	0x0258
U4C	RGNX	Ring cadence maximum total time in seconds multiplied by 2400.	0x6720

4.27.8 U4D MOD1

U4D is a bit-mapped register that controls various telephony functions including the enabling of calling and guard tones and loop current verification prior to dialing. All bits in this register are read/write except the reserved bits 15, 13, 9, 6, 2, and 0. These bits must not be written with a logic 1 and reading them returns a value of 0. Bit 14 (TOCT) = 0 (default) turns off Calling Tone after Answer Tone detection and allows Calling Tone cadence to complete before proceeding with connect sequence (per V.25). TOCT = 1 turns off Calling Tone 200 ms after Answer Tone detection begins. Bit 12 (NHFP) = 0 (default) disables hook-flash during pulse dialing (ignores & and ! dial modifiers). NHFP = 1 enables hook-flash during pulse dialing. Bit 11 (NHFD) = 0 (default) disables hook-flash during dial string (tone or pulse). NHFD = 1 enables hook-flash during (tone or pulse) dial string. Bit 10 (CLPD) = 0 (default) Modem ignores loop current prior to dialing. If CLPD = 1, modem measures loop current prior to dialing. This bit is used in conjunction with the loop current debounce registers U50 and U51 (LCDN and LCDF), and U4D bit 1 (LLC). U50 provides a delay between the modem going off-hook and the loop current measurement. The delay allows the loop current to stabilize prior to the measurement. Some countries require the presence of loop current prior to dialing. Bit 8 (FTP) = 0 (default) allows mixing tone and pulse dialing in a single AT command. FTP = 1 forces the first dialing mode encountered (tone or pulse) for the entire AT command. Bit 7 (SPDM) = 0 (default) causes the modem to pulse dial if an ATDP command is given. If this bit is set to 1 the pulse dial modifier, P, is ignored, and the dial command is carried out as a tone dial (ATDT). Bit 5 (GT18) = 0 (default) disables the 1800 Hz Guard tone. GT18 = 1 enables the 1800 Hz Guard tone. Bit 4 (GT55) = 0 (default) disables the 550 Hz Guard tone. GT55 = 1 enables the 550 Hz Guard tone. Bit 3 (CTE) = 0 (default) disables and CTE = 1 enables the Calling Tone referred to in bit 14 (TOCT). The Calling Tone is a 1300 Hz tone in originate mode with a 0.5–0.7 sec on/1.5–2.0 sec off cadence as described in V.25.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		TOCT		NHFP	NHFD	CLPD		FTP	SPDM		GT18	GT55	CTE			
Type		R/W		R/W	R/W	R/W		R/W	R/W		R/W	R/W	R/W			

Reset settings = 0x0000

Bit	Name	Function
15	Reserved	Read returns zero
14	TOCT	**Turn Off Calling Tone.** **0 =Disable.** 1 = Enable.
13	Reserved	Read returns zero
12	NHFP	**No Hook Flash Pulse.** **0 =Disable.** 1 = Enable.
11	NHFD	**No Hook Flash Dial.** **0 =Disable.** 1 = Enable.
10	CLPD	**Check Loop Current Before Dialing.** **0 = Ignore.** 1 =Check.
9	Reserved	Read returns zero.
8	FTP	**Force Tone or Pulse.** **0 =Disable.** 1 = Enable.
7	SPDM	**Skip Pulse Dial Modifier.** **0 =No.** 1 =Yes.
6	Reserved	Read returns zero
5	GT18	**1800 Hz Guard Tone Enable.** **0 =Disable.** 1 = Enable.
4	GT55	**550 Hz Guard Tone Enable.** **0 =Disable.** 1 = Enable.
3	CTE	**Calling Tone Enable.**
2:0	Reserved	Read returns zero

4.27.9 U4E Pre Dial delay time register

U4E sets the delay time between the ATD command carriage return and when the modem goes off-hook and starts dialing (either tone or pulse). This delay establishes the minimum time the modem must be on-hook prior to going off-hook and dialing. France, Sweden, Switzerland, and Japan have minimum on-hook time requirements. The value stored in U4E is the desired delay minus 100 ms. The 100 ms offset is due to a delay inherent in the dialing algorithm. The value stored in the register is a hexadecimal number with ms units. "Country Dependent Setup" on page 123, has information about country-specific values for this register.

Register	Name	Description	Default
U4E	PRDD	Pre-dial delay-time after ATD command that modem waits to dial (ms units). The modem stays on-hook during this time.	0x0000

Copyright Delta Design BVBA

4.27.10 U4F Flash Hook Time register

U4F sets the time the modem goes on-hook as a result of a “!” or”&” dial modifier (flash hook). The value stored in the register is a hexadecimal number with ms units.

Register	Name	Description	Default
U4F	FHT	Flash Hook Time. Time corresponding with “!” or “&” dial modifier that the SMD24XXL goes on-hook during a flash hook (ms units).	0x01F4

4.27.11 U50-U51 Loop Current Debounce registers

U50 (LCDN) sets the loop current debounce on-time, and U51 (LCDF) sets the loop current debounce off-time.
Loop current debounce is used in cases where the presence or absence of loop current must be determined prior to taking some action. For example, it may be desirable, or required, to verify the presence of loop current prior to dialing. The loop current debounce on-time, LCDN, is used to program a delay in measuring loop current after the modem goes off-hook to ensure the loop current is stable prior to the measurement. LCDN is used in conjunction with U4D[10] (CLPD) and U4D[0] (LCN). Loop current debounce off-time, LCDF, is used in conjunction with LCN to delay the modem going on-hook if loop current is interrupted during a connection. The values stored in the registers are hexadecimal numbers with ms units. The default value for LCDN is 350 ms. The default value for LCDF is 200 ms. The range of values for these registers is 0–65535 in ms units.

Register	Name	Description	Default
U50	LCDN	Loop current debounce on time (ms units).	0x015E
U51	LCDF	Loop current debounce off time (ms units).	0x00C8

4.27.12 U52 Transmit Level register

U52 (XMTL) adjusts the modem transmit level appearing on a 600 . line. The default value of 0x0000 results in a –9.85 dBm transmit level.
U52 can be used to decrease this level in 1 dBm units to the minimum modem receive threshold of –48 dBm with a register value of 0x0026.

Register	Name	Description	Default
U52	XMTL	Transmit level (1 dB units)—Sets the modem data pump transmitter level. Default level of 0 corresponds to –9.85 dBm. Transmit level = –(9.85 + XMTL) dBm. Range = –9.85 to –48.	0x0000

4.27.13 U53 MOD2

U53 (MOD2) is a bit-mapped register with all bits, except bit 15, reserved. The AT&H11 command sets the V.23 1200/75 bps mode. Bit 15 (REV) is used to enable V.23 reversing. This bit is set to 0 b (disable reversing) by default. Setting this bit to 1 b enables reversing transmit and receive speeds.
Reversing is initiated by the modem in the “origination mode” (low speed TX and high speed RX). U53 resets to 0x0000 with a power-on or manual reset.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REV															
Type																

Reset settings = 0x0000

Bit	Name	Function
15	REV	**V.23 Reversing.** **0 = Disable.** 1 =Enable.
14:0	Reserved	Read returns zero

4.27.14 U62 DAAC1

U62 (DAAC1) is a bit-mapped register with only bits 1, 2, and 8 available. All other bits in this register are reserved and must be set according to the table. U62 resets to 0x0804 with a power-on or manual reset.
Bit 1 (DL) = 1 or 0 causes digital loopback to occur beyond the ISOcap™ interface out to and including the analog hybrid circuit. Setting bit 1 to 1 enables digital loopback across the isolation barrier only. This setting is used in conjunction with the ATH and AT&T3 commands.
Bit 2 (FOH) controls when automatic Si3018/10 calibration takes place.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	1	0	0	OHS2	0	0	0	0	0	FOH	DL	0
Type								R/W						R/W	R/W	

Reset settings = 0x0804

Bit	Name	Function
15:12	Reserved	Must be set to 0.

Copyright Delta Design BVBA

11	Reserved	Must be set to 1.
10:9	Reserved	Must be set to 0.
8	OHS2	**On-Hook Speed 2.** This bit works in combination with the OHS bit (U67, bit 6) to set the on-hook speed. The on-hook speeds are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 Mean On-Hook Speed** 0 0 Less than 0.5 ms 0 1 3 ms ±10% (meets ETSI standard) 1 X 26 ms ±10% (meets Australia spark quenching spec)
7:3	Reserved	Must be set to 0.
2	FOH	**Fast Off-Hook.** 0 = Automatic Calibration Time set to 426 ms. **1 = Automatic Calibration Time set to 106 ms.**
1	DL	**Isolation Digital Loopback (see the AT&T commands).** **0 = Loopback occurs beyond the DAA interface, out to and including the analog hybrid circuit.** 1 = Enables digital loopback mode across isolation barrier only.
0	Reserved	Must be set to 0.

4.27.15 U63 DAAC3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									ACT[3:0]							
Type	R/W															

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns zero.
7:4	ACT[3:0]	**AC Termination Select.** **ACT[3:0] AC Termination** **0000 Real 600 Ω** 0011 220 Ω+ (820 Ω|| 120 nF) and 220 Ω + (820 Ω|| 115 nF) 0100 370 Ω + (620 Ω || 310 nF) 1111 Global complex impedance
3:0	Reserved	Read returns zero.

4.27.16 U65 DAAC4

U65 (DAAC4) is a bit-mapped register with bits 3:0 and 12:5 reserved. Bits 1:0 and 6:5 must not be changed in a read-modify-write cycle.
Bit 14 (PWMG) = 0 (default) provides 0 dB gain to AOUT. PWMG = 1 provides a 6 dB gain to AOUT. Not applicable to SMD24XXL
Bit 13 (PDN) = 0 allows the device to operate at normal power level. PDN = 1 completely powers down both the modem. The bit takes effect at the carriage return of the AT command writing this bit to a 1. Once this bit is set, the modem must be reset via the RESET pin to become active. When reset, the modem reverts to the default settings.
Bit 4 (PDL) = 0 (default) allows the modem to operate at normal power levels. PDL = 1 powers down the Si3018/10. This is a test mode typically used for board-level debugging, not normal modem operation.
U65 resets to 0x00E0 with a power-on or manual reset.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		PWMG	PDN									PDL				
Type		R/W	R/W									R/W				

Reset settings = 0x00E0

Bit	Name	Function
15	Reserved	Read returns zero
14	PWMG	**PWM Gain.** **0 =No gain.** 1 = 6 dB gain applied to AOUT. NOT APPLICABLE TO SMD24XXL
13	PDN	**Powerdown.** Completely powerdown the modem. Once set to 1, the SMD24XXL must be reset to power on. **0 = Normal.** 1 = Powerdown.
12:8	Reserved	Read returns zero.
7:5	Reserved	Must not change in a read-modify-write

Copyright Delta Design BVBA

4	PDL	**Powerdown Line-Side Chip.** **0 = Normal operation.** 1 = Places the Si3018 in powerdown mode.
3:0	Reserved	Must not change in a read-modify-write

4.27.17 U66 DAAC5

U66 (DAAC5) is a bit-mapped register with all bits except bit 6 reserved.
Bit 6 (FDT) is a read-only bit that reports whether or not an ISOcap™ frame lock is established. FDT is typically used for board-level debugging and is not used during normal modem operation.
U66 resets to 0x0040 with a power-on or manual reset assuming framelock is established.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name										FDT						
Type										R						

Reset settings = 0x0040

Bit	Name	Function
15:7	Reserved	Read returns zero
6	FDT	**Frame Detect.** 0 = Indicates ISOmodem® has not established frame lock. 1 = Indicates ISOmodem frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	Reserved	Do not modify.

4.27.18 U67 ITC1

International Configuration Registers include U67 through U6A. These are bit-mapped registers that control international configuration settings, such as dc and ac termination, ringer impedance and detection, current limit, and billing tone protection.

U67 is a bit-mapped register with bits 5:4, 8, 11:10, and 15:14 reserved. U67 resets to 0x0008 with a power-on or manual reset.
Bit 7 (DCR) is used to set the dc line termination of the modem. DCR = 0 b is the normal mode of operation with dc impedance selected by U67[3:2] (DCV). When DCR = 1 b , the device presents a dc line impedance of 800 ., which can be used to enhance operation with a parallel phone, for improved low line voltage performance and for overload protection. This bit *must* be set to 0 when the modem is on-hook. See "DC Termination" for details.
Bit 6 (OHS) is used to control the speed with which the modem drops the line. The default setting, OHS = 0 b , causes the modem to go from the off-hook state (drawing loop current) to the on-hook state (not drawing loop current) quickly.
This operation is acceptable in many countries. However, some countries, such as Italy, South Africa, and Australia, have spark quenching requirements. Spark quenching can be accomplished by placing a resistor and a capacitor across the hookswitch or by controlling the off-hook to on-hook transition speed to prevent excessive voltage build-up. Slowly reducing the loop current to zero fulfills the spark quenching requirement without the extra components. Setting OHS = 1 b causes the hookswitch to turn off the loop current with a ramp instead of a step.
Bits 3:2 (DCV) select the dc termination for the modem. DCV = 00 b is the lowest voltage mode supported on the SMD2493L/57/34/15/04. DCV = 01 b is the next lowest voltage mode. See "DC Termination" for details.
Bit 1 (RZ) = 0 (default) allows ringer impedance to be determined by external components. This impedance is typically 800–900 k. RZ = 1 enables on-chip synthesis of a lower ringer impedance for countries, such as Poland, South Africa, and South Korea.
Bit 0 (RT), Ring Threshold, is used to satisfy various country ring detect requirements. RT = 0 b (default) sets the ring threshold for 11–22 V RMS. RT = 1 b sets the ring threshold for 17–33 V RMS . Signals below the lower level of the range are not detected. Signals above the upper level of the range are always detected.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name			MINI[1:0]				ILIM		OFF	OHS			DCV[1:0]		RZ	RT
Type			R/W				R/W		R/W	R/W			R/W		R/W	R/W

Reset settings = 0x0008

Bit	Name	Function
15:14	Reserved	Read returns zero
13:12	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current at which the DAA can operate. Increasing the minimum operational loop current can improve signal headroom at a lower TIP/RING voltage. **MINI[1:0] Min Loop Current** **00 10 mA** 01 12 mA 10 14 mA 11 16 mA
11:10	Reserved	Read returns zero
9	ILIM	**Current Limiting Enable.** **0 = Current limiting mode disabled.** 1 = Current limiting mode enabled. This mode limits loop current to a maximum of 60 mA per the TBR21 standard.

Copyright Delta Design BVBA

8	Reserved	Read returns zero
7	OFF	**DC Impedance Selection.** **0 =50 Ω dc termination is selected. This mode should be used for all standard applications.** 1 = 800 Ω dc termination is selected.
6	OHS	**On-Hook Speed.** This bit works in combination with the OHS2 bit (U62, bit 8) to set the on-hook speed. The on-hook speeds are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 Mean On-Hook Speed** 0 0 Less than 0.5 ms 0 1 3 ms ±10% (meets ETSI standard) 1 X 26 ms ±10% (meets Australia spark quenching spec)
5:4	Reserved	Read returns zero
3:2	DCV[1:0]	**TIP/RING Voltage Adjust.** These bits adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage can improve signal headroom. **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V **10 3.35 V** 11 3.5 V
1	RZ	**Ringer Impedance.** **0 = Maximum (high) ringer impedance.** 1 = Synthesize ringer impedance
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level does not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. **0 = 11 to 22 V rms .** 1 = 17 to 33 V rms .

4.27.19 U68 ICT2

U68 is a bit-mapped register with bits 15:3 reserved. Reading these bits returns zero. Bits 4 and 2:0 are all read/write. Bit 2 (BTE) = 0 b (default) is disabled by default. When BTE = 1 b , the DAA automatically responds to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 b and BTD goes high, the dc termination is increased to 800 ohm to reduce loop current. If BTE and U70[9] (RIM) are set to 1 b , an interrupt from U70[1] (RI) also occurs when BTD goes to 1 b (high).
Bit 1 (ROV) is normally 0 b and is set to 1 b to report an excessive receive input level. ROV is cleared by writing it to 0 b .
Bit 0 (BTD) = 0 b normally but is set to 1 if a billing tone is detected. BTD is cleared by writing a 0 b to BTD. U68 resets to 0x0000 with a power-on or manual reset.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														BTE	ROV	BTD
Type														R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:3	Reserved	Do not modify.
2	BTE	**Billing Tone Protect Enable.** **0 = Disabled.** 1 = Enabled. When set, the DAA responds automatically to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the dc termination is released (800 Ω presented to line). If BTE and RIM (U70, bit 9) are set, an RI (U70, bit 1) interrupt also occurs when BTD goes high.
1	ROV	**Receive Overload.** The bit is set when the receive input (i.e., receive pin goes below ground) has an excessive input level. This bit is cleared by writing a 0 to this location. **0 = Normal receive input level.** 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit is set if a billing tone is detected. This bit is cleared by writing a 0 to this location. 0 = No billing tone. 1 = Billing tone detected.

4.27.20 U6A ICT4

U6A (ITC4)

U6A is a bit-mapped register with bits 15:3 and 1:0 reserved. Reading these bits returns zero. Bit 2 is read only. Bit 2 (OVL) is a read-only bit that detects a receive overload. This bit is similar to U68[1] (ROV) except OVL clears itself after the overload condition is removed.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														OVL		
Type														R		

Reset settings = N/A

Bit	Name	Function
15:3	Reserved	Read returns zero.
2	OVL	**Overload Detected.** This bit has the same function as ROV, but clears itself after the overload has been removed.
1:0	Reserved	Do not modify.

4.27.21 U6C LVS

U6C contains the line voltage status register, LVS, and resets to 0x0000. Bits 7:0 are reserved, and a read returns zero.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LVS[7:0]															
Type	R															

Reset settings = 0x0000

Bit	Name	Function
15:8	LVS[7:0]	**Line Voltage Status.** Eight bit signed, twos complement number representing the tip-ring voltage. Each bit represents 1 V. Polarity of the voltage is represented by the MSB (sign bit). 0000_0000 = Measured voltage is < 3 V.
1:0	Reserved	Read returns zero.

4.27.22 U6E CK1

U6E controls the clockout divider. Bits 15:13 and 7:0 are reserved. U6E resets to 0x1F20 with a power-on or manual reset. Bits[12:8] (R1) make up the R1 clockout divider. A 81.92 MHz (SMD2404L/15) or 98.304 MHz (SMD2434L/57) clock signal passes through a ÷(R 1 +1) circuit to derive the CLKOUT signal on of the SMD2493L/57/34/15/04. If R1 = 00000 b , CLKOUT is disabled. R1 is set at a default value of 11111 b resulting in CLKOUT = 3.072 MHz (SMD2434L/57) or CLKOUT = 2.56 MHz (SMD2404L/15).

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				R1[4: 0]												
Type				R/W										R		

Reset settings = 0x1F20

Bit	Name	Function
15:13	Reserved	Do not modify.
12:8	R1[4: 0]	**R1 CLKOUT Divider** 0 CLKOUT off. R1 R1 + 1 (default R1 = 31; 2.4576 MHz). R1 = 31 required for proper codec interface operation.
7:0	Reserved	Read returns zero.

4.27.23 U70 IO0

U70 controls escape and several indicator and detector masks and provides several read-only status bits.
Bits 5, 6, 7, and 14 are reserved.
Bits 4:0 are read only, and bits 15 and 13:8 are read/write. U70 resets to 0x2700 with a power-on or manual reset.
Bit 15 (HES) = 0 b (default) disables the hardware escape pin (SMD2493L/57/34/15/04,DTR/ESC). Setting HES = 1 b enables ESC. When ESC is enabled, escape from the data mode to the command mode occurs at the rising edge of the ESC pin. Multiple escape options can be enabled simultaneously. For example, U70[13] (TES) =1 b by default, which enables the “+++” escape. If HES is also set (HES = 1 b), either escape method works. Additionally, the 9th bit escape can also be enabled with the AT\B6 command or through autobaud.
Bit 13 (TES) = 1 b (default) enables the traditional “+++” escape sequence. To successfully escape from data mode to command mode using “+++”, there must be no UART activity for a guard period, determined by register S12, both before and after the “+++”. S12 can be set for a period ranging from 200 ms to 5.1 seconds.
Bit 12 (CIDM) = 0 b (default) prevents a change in U70[4] (CID), caller ID, from triggering an interrupt. If CIDM = 1 b , an interrupt is triggered with a low-to-high transition on CID.
Bit 11 (OCDM) = 0 b (default), an interrupt is not triggered with a change in OCD. If OCDM = 1 b a low-to-high transition on U70[3] (OCD), overcurrent detect, triggers an interrupt. This bit must be set for Australia and Brazil.

Bit 10 (PPDM) = 1 b (default) causes a low-to-high transition in U70[2] (PPD), parallel phone detect, to trigger an interrupt. If PPDM = 0 b , an interrupt is not triggered with a change in PPD.
Bit 9 (RIM) = 1 b (default) causes a low-to-high transition in U70[1] (RI), ring indicator, to trigger an interrupt. If RIM = 0 b , an interrupt is not triggered with a change in RI.
Bit 8 (DCDM) = 1 b (default) causes a high-to-low transition in U70[0] (DCD), data carrier detect, to trigger an interrupt. If DCDM = 0 b , an interrupt is not triggeredwith a change in DCD.
Bits 4:0 are the event indicators described below. All are "sticky" (i.e., remain set to 1 b after the event) and clear on an interrupt read (AT:I).

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W

Reset settings = 0x2700

Bit	Name	Function
15	HES	**Hardware Escape Pin. (DTR)** **0 = Disable.** 1 = Enable.
14	Reserved	Read returns zero.
13	TES	**Enable "+++" Escape.** 0 =Disable. **1 =Enable.**
12	CIDM	**Caller ID Mask.** **0 = Change in CID will not affect INT.** 1 = A low to high transition in CID activates INT.
11	OCDM	**Overcurrent Detect Mask.** **0 = Change in OCD does not affect INT.** ("X" result code is not generated in command mode.) 1 = A low to high transition in OCD will activate INT. ("X" result code is generated in command mode.)
10	PPDM	**Parallel Phone Detect Mask.** 0 = Change in PPD does not affect INT. **1 = A low to high transition in PPD will activate INT.**
9	RIM	**Ring Indicator.** 0 = Change in RI does not affect INT. **1 = A low to high transition in RI activates INT.**
8	DCDM	**Data Carrier Detect Mask.** 0 = Change in DCD does not affect INT. 1 = A high to low transition in DCD (U70, bit 0), which indicates loss of carrier, activates INT.
7	Reserved	Must be set to zero.
6:5	Reserved	Read returns zero
4	CID	**Caller ID (sticky).** Caller ID preamble has been detected; data will soon follow. Clears on :I read.
3	OCD	**Overcurrent Detect (sticky).** Overcurrent condition has occurred. Clears on :I read.
2	PPD	**Parallel Phone Detect (sticky).** Parallel phone detected since last off-hook event. Clears on :I read.
1	RI	**Ring Indicator.** Active high bit when the modem is on-hook, indicates ring event has occurred. Clears on :I read.
0	DCD	**Data Carrier Detect (status).** Active high bit indicates carrier detected (equivalent to inverse of DCD pin).

4.27.24 U71 IO1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												COMP				PRT
Type												R/W				R/W

Reset settings = 0x0000

Bit	Name	Function
15:5	Reserved	Read returns zero.
4	COMP	**P0 = Disables compression (PCM mode).** 1 = Enables linear compression.
3:1	Reserved	Read returns zero.
0	PRT	**0 = Disables PCM mode.** 1 = Enables PCM mode.

4.27.25 U76 GEN1

Copyright Delta Design BVBA

U76 provides control for parallel phone detect (PPD) intrusion parameters including the off-hook sample rate (OHSR), absolute current level with modem off-hook (ACL), ACL update from LVCS (FACL), and the difference in current between ACL and LVCS that trigger an off-hook intrusion detection (DCL). All bits in U76 are read/write.
OHSR[15:9] sets the off-hook loop current sample rate for intrusion algorithms in 40 ms units. The default value is 25 (1 sec). The minimum recommended value is 5 (260 ms). The sample rate can be adjusted to much lower values; however, the likelihood of false intrusion detections increases sharply with sample rates less than 520 ms.
Bit 8 (FACL). If FACL = 0 b (default), the ACL register is automatically updated to the LVCS value at the sample rate determined by OHSR. This feature is used to ensure the ACL value is continuously updated. Updating ACL allows host software to determine the loop current (value returned in ACL) provided the modem is off-hook longer than the time defined by U77(IST). Loop current on a particular line can vary over time due to a variety of factors including temperature and weather conditions. Updating ACL reduces the probability of false intrusion detection by ensuring the ACL reference reflects the most recent off-hook conditions. If FACL = 1 b , a value can be written into ACL by the host. This value is not updated and remains in the ACL register until overwritten by the host or until FACL is returned to 0 and updates from LVCS overwrite the stored value. Writing an initial value to ACL eliminates the possibility of the modem going off-hook for the first time simultaneously with an intrusion and storing the intrusion loop current in ACL.
Bits 7:5 (DCL) set the differential level between ACL and LVCS that triggers an off-hook PPD interrupt. DCL is adjustable in 3 mA units. The default value is 2 (6 mA).
Bits 4:0 (ACL): ACL provides a means of detecting a parallel phone intrusion during the time between the modem going off-hook and the U77[15:12] (IST) time value. If ACL = 0, the modem has no reference and must use the loop current sample from the first off-hook event as a reference for parallel phone intrusion detection. Typically, the host sets ACL to an approximate value and FACL = 0 before the first off-hook event after powerup or reset. This allows the updated ACL value to be used for subsequent calls and eliminates a potential detection problem if an intrusion occurs simultaneously when the modem goes off-hook for the first time after a powerup or reset. If ACL = 0 b , it is ignored by the off-hook intrusion algorithm. A PPD interrupt is generated if U79[4:0] (LVCS) is DCL less than ACL for two consecutive samples. The modem writes ACL with the contents of LVCS after an intrusion with the last LVCS value before the intrusion. The default value for ACL is 0 b .
U76 resets to 0x3240 with a power-on or manual reset.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OHSR[6:0]							FACL	DCL[2:0]			ACL[4:0]				
Type	R/W							R/W	R/W			R/W				

Reset settings = 0x3240

Bit	Name	Function
15:9	OHSR[6:0]	**Off-Hook Sample Rate (40 ms units).** Sets the sample rate for the off-hook intrusion algorithms (1 second default).
8	FACL	**Force ACL.** **0 = While off-hook, ACL is automatically updated with LVCS.** 1 = While off-hook, ACL does not change from the value written to it while on-hook.
7:5	DCL[2:0]	**Differential Current Level (3 mA units).** Sets the differential level between ACL and LVCS that will trigger an off-hook PPD interrupt (default = 2).
4:0	ACL[4:0]	**Absolute Current Level (3 mA units).** ACL represents the value of LVCS current when the ISOmodem® is off-hook and all parallel phones are on-hook. If ACL = 0, then it is ignored by the off-hook intrusion algorithm.The ISOmodem will also write ACL with the contents of LVCS before an intrusion and before going on-hook (default = 0).

4.27.26 U77 GEN2

U77 is a bit-mapped register that controls parameters relating to intrusion detection and overcurrent detection. U77 resets to 0x401E with a power-on or manual reset.
Bits 15:12 (IST) set the delay between the time the modem goes off-hook and the intrusion detection algorithm begins. This register has 250 ms increments, and the default value is 4 (1 sec).
Bit 11 (HOI) determines whether the host or modem responds to an intrusion. HOI = 0 b (default) prevents the modem from hanging-up in response to an intrusion without host intervention. In this case, the host monitors U70[2] (PPD) and takes the appropriate action when PPD is asserted indicating an intrusion. If HOI = 1 b , the modem hangs up immediately when an intrusion is detected without host intervention. If %V N commands are set, HOI also causes the “LINE IN USE” result code upon PPD interrupt.
Bit 9 (AOC) = 0 b (default) disables AutoOvercurrent. If enabled and an overcurrent condition is detected, the dc termination switches to 800 ., thus, reducing the current. If AOC = 0, the overcurrent condition is only reported by U70[3] (OCD).
Bits 8:0 (OHT) set the delay between the time the modem goes off-hook and LVCS is read for an overcurrent condition. The default value for this register is 16 ms.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IST[3:0]				HOI		AOC	OHT[8:0]								
Type	R/W				R/W		R/W	R/W								

Reset settings = 0x401E

Bit	Name	Function

Copyright Delta Design BVBA

15:12	IST[3:0]	**Intrusion Settling Time (250 ms units).** Delay between when the ISOmodem® goes off-hook and the off-hook intrusion algorithm begins. Default is 1 s.
11	HOI	**Hang-Up On Intrusion.** **0 = ISOmodem will not automatically hang up when an off-hook PPD interrupt occurs.** 1 = ISOmodem automatically hangs up on a PPD interrupt. If %Vn commands are set, HOI also causes the “LINE IN USE” result code upon PPD interrupt.
10	Reserved	Read returns zero.
9	AOC	AOC**Overcurrent Protection.** Enable Overcurrent protection. **0 = Disable.** 1 = Enable. **Note:** AOC may falsely detect an overcurrent condition in the presence of line reversals or other transients. Therefore, this feature should not be used in applications or locations (such as Japan) where line reversals are common or may be expected.
8:0	OHT[8:0]	**Off-Hook Time (1 ms units).** Time before LVCS is checked for overcurrent condition after going off-hook (30 ms default).

4.27.27 U78 GEN3

U78 is a bit-mapped register that controls intrusion detection blocking and intrusion suspend. U78 resets to 0x0000 with a power-on or manual reset.
Bits 15:14 (IB) controls intrusion blocking after dialing has begun.
Bits 7:0 (IS) set the delay between the start of dialing and the start of the intrusion algorithm when IB = 10 b .

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IB[1:0]								IS[8:0]							
Type	R/W								R/W							

Reset settings = 0x0000

Bit	Name	Function
15:14	IB[1:0]	**Intrusion Blocking.** Defines the method used to block the off-hook intrusion algorithm from operation after dialing has begun. **0 = No intrusion blocking.** 1 = Intrusion disabled from start of dial to end of dial. 2 = Intrusion disabled from start of dial to IS register time-out. 3 = Intrusion disabled from start of dial to connect (“CONNECT XXX”, “NO DIALTONE”, or “NO CARRIER”).
13 :8	Reserved	Read returns zero.
7:0	IS[8:0]	**Intrusion Suspend (500 ms units).** When IB = 2, this register sets the length of time from when dialing begins that the off-hook intrusion algorithm is blocked (suspended) (default = 00000000 b).

4.27.28 U79 GEN4

U79 is a bit-mapped register. Bits 15:5 are reserved. Bits 4:0 represent the line voltage, loop current, or on-hook line monitor. While the modem is on-hook, the value in the LVCS register measures loop voltage. This value can be used to determine if a line is connected or if a parallel phone or other device goes off-hook or on-hook. The accuracy of the LVCS bits is ±20%. When the modem goes off-hook, the value in the LVCS register measures loop current. LVCS can indicate when a parallel phone or other device goes on-hook or off-hook and detect whether enough loop current is available for the modem to operate or if an overload condition exists.
The line voltage monitor full scale may be modified by changing R5 as follows:
V MAX =V MIN + 4.2 (10M + R5 + 1.78k)/(R5 +1.78k)/5 U69[2] (MODE) must be set to 1 b prior to reading LVCS while the modem is on-hook. U69[2] (MODE) must be disabled (MODE = 0 b) before the modem can go off-hook, dial, or answer a call.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												LVCS[4:0]				
Type												R/W				

Reset settings = 0x0000

Bit	Name	Function
15:5	Reserved	Read returns zero.
4:0	LVCS[4:0]	**Line Voltage Current Sense.** Represents either the line voltage, loop current, or on-hook line monitor. **On-Hook Voltage Monitor (2.75 V/bit ±20%).**

Copyright Delta Design BVBA

		00000 = No line connected. 00001 = Minimum line voltage (V MIN =3.0V ± 0.5 V). 11111 = Maximum line voltage (87 V ± 20%). The line voltage monitor full scale may be modified by changing R5 as follows: V MAX = V MIN + 4.2 (10M + R5 + 1.6k)/(R5 +1.6k)/5 **Off-Hook Loop Current Monitor (3 mA/bit).** 00000 = No loop current. 00001 = Minimum loop current. 11110 = Maximum loop current. 11111 = Loop current is excessive (overload). Overload > 140 mA in all modes except TBR21 Overload > 54 mA in TBR21 mode

4.27.29 U7A GENA

U7A is a bit-mapped register. U7A resets to 0x0000.
Bits 15:8 and 5:3 are reserved.
Bit 7 (DOP) is used in a method to determine whether a phone line supports DTMF or pulse only dialing. See "Pulse/Tone Dial Decision" for details.
Bit 6 (ADD) attempts DTMF dial, then falls back to pulse dialing if unsuccessful. First digit is dialed as DTMF. If a dialtone is still present after two seconds, the SMD2493L/57/34/15/04 redials the first digit and remaining digits as pulse. If a dialtone is not present after two seconds, the SMD2493L/57/34/15/04 dials the remaining digits as DTMF.
Bit 1 (HDLC) controls whether the normal asynchronous mode (default) is used or the transparent HDLC mode is enabled. (See "Legacy Synchronous DCE Mode/Synchronous Access Mode" for more details on these modes.)
Bit 0 controls whether the normal ITU/Bellcore modem handshake (default) or a special fast connect handshake is used. Fast connect is typically used in specialized applications such as point-of-sale terminals where it is important to rapidly connect and transfer a small amount of data.

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name									DOP	ADD				V22HD	HDLC	FAST
Type									R/W	R/W				R/W	R/W	R/W

Reset settings = 0x0000

Bit	**Name**	**Function**
15:8	Reserved	Read returns zero.
7	DOP	**Dial or Pulse.** **0 = Normal ATDTW operation** 1 = Use ATDTW for Pulse/Tone Dial Detection (see also ATDW command)
6	ADD	**Adaptive Dialing** 1 = Enable **0 =Disable** Attempt DTMF dial, then fall back to pulse dialing if unsuccessful. First digit is dialed as DTMF. If a dialtone is still present after two seconds, the SMD249XX will redial the first digit and remaining digits as pulse. If a dialtone is not present after two seconds, the SMD24XXL will dial the remaining digits as DTMF.
5:3	Reserved	Read returns zero.
2	V22HD	**V.22bis Synchronous Mode.*** **0 = Normal asynchronous mode.** 1 = Transparent HDLC mode.
1	HDLC	**Synchronous Mode.*** **0 = Normal asynchronous mode.** 1 = Transparent HDLC mode.
0	FAST	**Fast Connect.*** **0 = Normal modem handshake timing per ITU/Bellcore standards.** 1 = Fast connect modem handshake timing.
***Note:** When V22HD, HDLC, or FAST bits are set, \N0 (wire mode) must be used.		

4.27.30 U7C GENC

U7C is a bit-mapped register with bits 15:5 and bits 3:1 reserved. U7C resets to 0x0000 with a power-on or manual reset.
Bit 4 (RIGPO) is output on RI (SMD2493L/57/34/15/04) when U7C[0] (RIGPOEN) = 1 b . This allows the RI pin to be configured as a general-purpose output pin under host processor control.
Bit 0 (RIGPOEN)=0 (default) allows RI (SMD2493L/57/34/15/04 pin 15) to indicate a valid ring signal. When Bit 0 =1 b , RI outputs the value of RIGPO.

Bit	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Name												RIGPO				RIGPOEN
Type																R/W

Reset settings = 0x0000

Copyright Delta Design BVBA

Bit	Name	Function
15:5	Reserved	Read returns zero.
4	RIGPO	**RI** RI (pin 16) follows this bit when RIGPIOEN = 1 b .
3:1	Reserved	Read returns zero.
0	RIGPOEN	**0 = RI indicates valid ring signal. (Normal ring-indicator mode)** 1 =RI (Pin 16) can be used as a general purpose output and follows U7C[4] (RIGPO).

4.27.31 U7D GEND

U7D is a bit-mapped register with bits 15:11 and bits 8:2 reserved. U7D resets to 0x0000 with a power-on or manual reset. Bit 1 (ATZD) = 0 (default) allows the ATZ command to be active. When Bit 1 = 1b, the ATZ command is disabled. Bit 0 (FDP) = 0 (default). FSK data processing stops when the carrier is lost. Unprocessed data is lost. Setting Bit 0 = 1 causes FSK data processing to continue for up to two bytes of data in the pipeline after carrier is lost.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name															ATZD	FDP
Type															R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:2	Reserved	Read returns zero.
1	ATZD	**ATZ Disabl e.** **0 = ATZ functions normally.** 1 = Disable ATZ command.
0	FDP	**FSK Data Processing.** **0 = FSK data processing stops when carrier is lost.** 1 = FSK data processing continued for 2 bytes after carrier is lost.

4.27.32 U87 SAM

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name						MINT	SERM	FSMS	XMTT							
Type						R/W	R/W	R/W	R/W							

Reset settings = 0x0000

Bit	Name	Function
15:11	Reserved	Read returns zero.
10	MINT	**Minimal Transparency** **0 = Generates two-byte <EM> transparency sequences.** This option will use codes <EM><T5> through <EM><T20>, if possible, for received data containing two back-to-back bytes requiring transparency. 1 = Generates one-byte <EM> transparency sequences. This option will only use codes <RM><T1> through <EM><T4> for received data.
9	SERM	**Special Error Reporting Mode** **0 = Ignore unrecognized in-band commands.** 1 = Generate <EM><0x45> (“E” for error) in response to any unrecognized in-band commands.
8	FSMS	**Framed Sub-Mode Startup** **0 = Upon successful connection, enter Transport Sub-Mode.** An <EM><FLAG> is required to enter Framed Sub-Mode. **1 = Upon successful connection, immediately enter Framed Sub-Mode.** The first received <EM><err> from a successful hunt is transformed into an <EM><flag>.
7:0	XMTT	**Transmitter Threshold** This value represents the number of bytes before a transmission is started. The following values are special: 0 The same as ten. Upon receipt of ten bytes, data is transferred. The DTE must supply a closing flag within the required time or an underrun will occur. 255 The same as infinity, e.g. never start a packet until the closing flag is received.

4.27.33 UAA V.29 Mode

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Copyright Delta Design BVBA

Name															V29ENA	
Type															R/W	

Reset settings = 0x0000

Bit	Name	Function
15:2	Reserved	Read returns zero.
1	V29ENA	**A0 = Disables V.29** 1 = Enables V.29
0	Reserved	Read returns zero.

Copyright Delta Design BVBA

5 APPLICATION NOTES

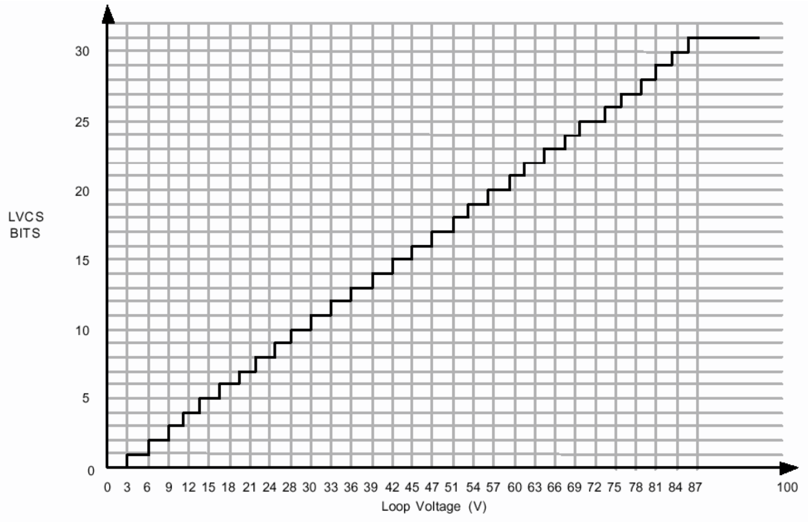
5.1 VOLTAGE MONITORING

The line voltage value can be read from register U79(LVCS)[4:0].

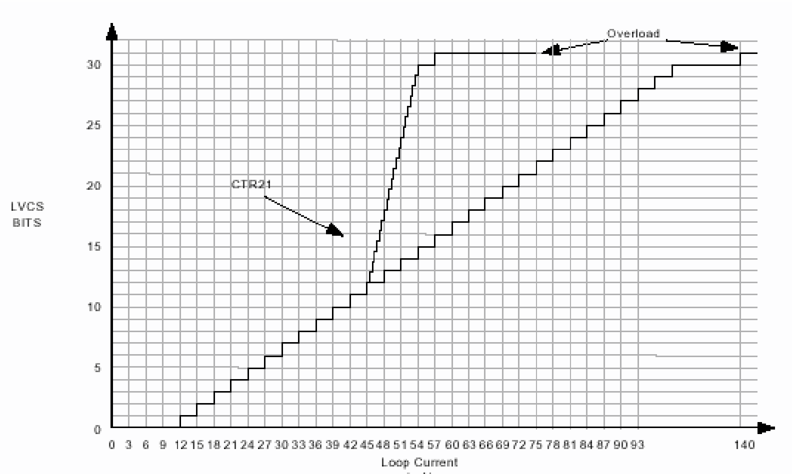
The modem has the ability to measure both line voltage and loop current. The 8-bit LVCS register, U79(LVCS) [7:0], reports line voltage measurements when on-hook and loop current measurements when off-hook. Using the LVCS bits, the user can determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- Detect if there is an overload condition that could damage the DAA (see overload protection feature).

Line Voltage Measurement
The modem reports the on-hook line voltage with the LVCS bits. LVCS has a full scale of 87 V with an LSB of 3 V. The first code (0 →1) is skewed such that a 0 indicates the line voltage is < 3 V.
The accuracy of the LVCS bits is ±10%. The user can read these bits directly through the LVCS register. A typical transfer function is shown in the figure below.



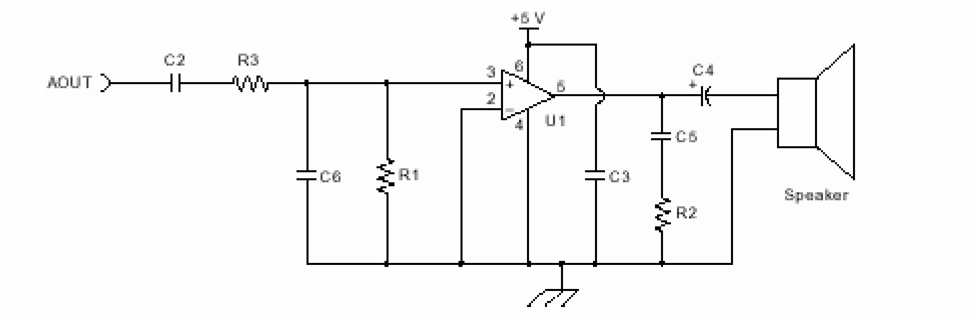
Loop Current Measurement
When the modem is off-hook, the LVCS bits measure loop current in 3.3 mA/bit resolution. These bits enable the user to detect another phone going off-hook by monitoring the dc loop current. The line current sense is detailed in the figure below.



Copyright Delta Design BVBA

5.2 ANALOG OUTPUT

The figure below illustrates an optional application circuit to support the analog output capability of the modem for call progress monitoring purposes.



Symbol	Value
C2, C3, C5	0.1 µF, 16 V, ±20%
C4	100 µF, 16 V, Elec. ±20%
C6	820 pF, 16 V, ±20%
R1	10 kΩ, 1/10 W, ±5%
R2	10 Ω, 1/10 W, ±5%
R3	47 kΩ, 1/10 W, ±5%
U1	LM386

5.3 FAST CONNECT

The SMD2493L/57/34/15/04 supports several fast connect modes of operation to reduce the time of a connect sequence in originate mode.

V.29 Fast Connect

In addition to the low modulation speed fast connect modes, the modem (only SMD2457L/34/15) also supports a fast connect mode based on the 9600 bps V.29 fax modulation standard. In order to provide a time-critical interface from the host to the modem (only SMD2457L/34/15), the ISOmodem uses an interface derived from the fax class 1 AT command set. The example below shows how the class 1 AT commands for V.29 would commonly be used in a client-side terminal (originating modem).

Calling Modem Example:

♦ AT+FCLASS=1

Set the modem in fax mode so that it can be switched back and forth between Data and Command mode after executing AT FAX commands.

♦ AT:UAA,2

Disable normal fax tone during handshaking indicating to answer modem that V.29 fast connect will be requested. Cause the execution of AT+FTM = 2 at the beginning of connection.

♦ ATDT1234567

Dial the number and wait for <CONNECT> and<OK> to establish connection.

♦ AT+FTM=2 (For reference only; there is no need to send this command to the modem)

Transmit V.21(980 Hz) tone until Answer Tone(2100/ 2225 Hz) is received for 100 ms, followed by <OK>.

♦ AT:UAA,0

Restore UAA to default value.

♦ AT+FRM=96

Put modem in V.29 receiving mode. Wait for <CONNECT> and then receive data. Wait for <NO CARRIER>.

♦ AT+FTM=96

Set modem to V.29 transmit mode and wait for <CONNECT>. Send Data from DTE to DCE and wait for <OK> after sending <DLE><ETX> characters where DLE is a 0x10 character and ETX is a 0x03 character.

♦ AT+FRM=95

Set modem to V.29 short synchronous receiving mode. Wait for <CONNECT> and then receive data.
Wait for <NO CARRIER> indicating transmission has ended.

♦ AT+FTM=95

Send out short synchronous signal and wait for <CONNECT>. Send Data from DTE to DCE and wait for <OK> after sending <DLE><ETX> characters.

♦ ATH

Hang up the modem.

Copyright Delta Design BVBA

5.4 LEGACY SYNCHRONOUS DCE MODE/ SYNCHRONOUS ACCESS MODE

The SMD2493L/57/34/15/04 supports two different DTE interfaces to implement an Asynchronous DTE to Synchronous DCE conversion.
The table provides high-level options to choose between the Legacy Synchronous DCE Mode and the newer Synchronous Access Mode.

Synchronous Mode	U-Register	AT+ES Settings
Neither	U7A[2] = 0	+ES = D,,D
Leagacy Synchronous DCE Mode	U7A[2]=1	+ES=D,,D
Synchronous Access Mode		+ES=6,8

The Synchronous Access Mode has additional features compared against the Legacy Synchronous DCE Mode. For new designs, use the newer Synchronous Access Mode interface. Otherwise, if there is existing software written with the Legacy Synchronous DCE Mode interface, no software changes are required as long as the AT+ES command settings are not changed from the default value.

5.4.1 Legacy Synchronous DCE mode

As shown in the table , this Legacy Synchronous DCE Mode is chosen as long as the AT+ES setting is set to its default value of +ES = D,,D.
The fast connect transparent HDLC modes are enabled via U7A and require wire mode operation (\N0). Each of the stages (answer tone detect time, unscrambled ones detect time, etc.) in the connect sequence may be shortened. The amount that each of these are shortened when in fast connect mode depends on the modulation. The "transparent HDLC" mode of operation operates with an asynchronous DTE and a synchronous DCE. The SMD2493L/57/34/15/04 performs HDLC frame packing and unpacking, frame opening and closing, flag generation and detection, CRC computation and checking, and 0 insertion and deletion. To use this mode, the DTE rate must be greater than the DCE rate; flow control via either CTS or /Q and /S must be used and wire mode operation (\N0)
is required.

Protocol	DCE	Register Settings
All	Normal, Asynchronous	&Hn,\N0, AT+ES=D,,D
V.22, Bell212,V.22bis	Normal Transparent HDLC	&H6, 7, 8,\N0, U7A=0002, AT+ES=D,,D
Bell103, V.21	Fast connect, Asynchronous	&H9,10,\N0, U7A=0001, AT+ES=D,,D
V.22, Bell212	Fast connect, Asynchronous	&H7,\N0, U7A=0001, AT+ES=D,,D
V.22, Bell212	Fast connect, Transparent HDLC	&H7,\N0, U7A=0003, AT+ES=D,,D
V.22bis	Transparent HDLC	&H6,\N0, U7A=0002, AT+ES=D,,D

On the transmit side, if no data is received on TXD, the SMD2493L/57/34/15/04 continually transmits HDLC flags at the DCE. As soon as there are 10 characters sent into the transmit buffer, the SMD2493L/57/34/15/04 begins an HDLC frame at the DCE. The reason for this 10-character “head start” is to reduce the likelihood of an underrun once the HDLC frame has begun at the DCE.
As long as the host continues to send data, the SMD2493L/57/34/15/04 continues to zero insert, update the CRC value, and send data within an HDLC frame. To properly end the frame, the host must send a /Zn (see Table) indicating to the SMD2493L/57/34/15/04 the end of the frame. Once the SMD2493L/57/34/15/04 encounters the /Zn, it computes and sends the final CRC and begins transmitting HDLC flags. If an HDLC frame is smaller than the 10-character “head start”, the HDLC frame is started at the DCE upon receipt of the /Zn character. The /Tn metacharacter is sent to the host to provide an indication that an HDLC frame was sent successfully.

The “n” in the /Zn and /Tn is a single-byte, host-defined tag that can be used to track multiple HDLC frames. To facilitate transmit flow control, the modem sends the /S and /Q metacharacters to the host. If the transmit buffer (512 bytes) is three quarters full, the /S metacharacter is sent to the host. The host must then stop transmitting. When the transmit buffer empties down to half full, the /Q metacharacter is sent to the host to indicate that it is okay to begin transmitting again. If a transmit underrun occurs, the current frame is aborted, and a /Un is sent to the host. All data from the underrun to the receipt of the /Zn metacharacter is discarded by the modem. A design goal of the host software should be to eliminate any occurrence of the / Un metacharacter.
Because the “/” is an escape character, the host must send a “//” when a “/” appears in the transmit data stream. The SMD2493L/57/34/15/04 removes one “/” for each instance of “//” that appears on TXD.
On the receive side, as long as HDLC flags are received by the SMD2493L/57/34/15/04 at the DCE, it does not pass the data out RXD. Once the first non-flag word is detected, the SMD2493L/57/34/15/04 performs zero deletion, calculates the CRC value, and passes the data out RXD. The SMD2493L/57/34/15/04 continues in this manner until detecting the HDLC flags, which indicate the end of the frame. At this point, the HDLC frame is complete, and the SMD2493L/57/34/15/04 calculates the final CRC and compares it to the CRC value received in the frame. If the CRC matches, the SMD2493L/57/34/15/04 passes /G to the host. If the CRC does not match, the SMD2493L/57/34/15/04 passes /B to the host to initiate a retransmit request. Because the / is an escape character, the SMD2493L/57/34/15/04 sends a // when a / appears in the receive data stream. The host must remove one / for each instance of // that appears on RXD. Table lists additional escape characters that are used to control the flow of data between the SMD2493L/57/34/15/04 and the host in the "transparent HDLC" mode.

Character *	Direction	Description
/Zn	TX	Follows the last character of a transmit frame. Once the frame has been sent, a /T metacharacter is sent to the host. *n* denotes a frame tag. *n* is echoed back later with the /U or /T metacharacters to

Copyright Delta Design BVBA

		make frame tracking easier.
//	TX	A forward slash character is to be transmitted.
/E	TX	Escape back to command mode. SMD2493L/57/34/15/04 returns to command mode.
/Un	RX	A transmit underrun has occurred, but a /Z metacharacter was not received. When an underrun occurs, the current frame is aborted; a /*Un* is sent to host, where *n* is the frame tag. All data following the underrun, up to the /Z metacharacter, is discardedby the modem.
/Tn	RX	The transmit frame, n, has been sent. The *n* from the /Z is echoed with the /*Tn* to allow tracking frames.
/G	RX	The previous receive frame CRC check was successful.
/B	RX	The previous receive frame CRC check was unsuccessful.
/S	RX	Transmit buffer is almost full; the host must pause transmission to prevent an over-flow. If hardware flow control is used, the host may ignore this metacharacter.
/Q	RX	The host may begin transmitting again after a /S (pause) has been sent. If hardware flow control is used, the host may ignore this metacharacter.
//	RX	A forward slash character was received.
/A	RX	Receive frame aborted.
***Note:** Characters after "/" must be uppercase.		

5.4.2 Synchronous access mode

The Synchronous Access Mode is chosen by using the AT+ES=6,,8 command setting.
When using the Synchronous Access Mode, it is expected that the AT\N0 command be used to disable all other error correction protocols that may interfere with Synchronous Access Mode operation.
The Synchronous Access Mode has two distinct submodes. Switching between these two submodes can be accomplished within the confines of the same connection through the use of In-Band commands.

- Transparent Submode
- Framed Submode

The Transparent Submode creates a direct bit-by-bit translation from the DTE to and from the DCE. Any application that requires a method of reconstructing a serial bit-stream at the DCE can use the Transparent Sub-mode.
The Framed Sub-mode represents data at the DCE in HDLC/SDLC frames. This submode is typically used in Point-of-Sale Terminal Applications. A common feature used in conjunction with the Framed Submode is the use of the 16-bit CRC. When used with the CRC option, the Framed Submode can be used in the same applications currently using the Legacy Synchronous DCE Mode.
Prior to sending the ATDT to establish a SynchronousAccess Mode connection, the following commands and registers will require initialization: +MS, +ES, +ESA,+ITF, +IFC, U87 and U7A.
As an example, the closest equivalent to the Legacy Synchronous DCE Mode is the following initialization setting.

AT\N0	Required to disable MNP,V42 and other protocols
AT+ES=6,,8	Enable Synchronous Access Mode on originate or answer
AT+ESA=0,0,0,,1,0	Send Abort on underrun/overrun in Framed Submode. Enable CRC generation and checking.
AT+IFC=2,2	CTS/RTS Flow Control
AT+ITF=0383,0128	Controls CTS Flow Control Thresh-old. CTS off at 383 bytes, CTS On at 128 bytes.
AT:U87,010A	Direct to Framed Sub-mode upon connection. DCE starts to transmit upon receipt of 10 bytes from the DTE.

In addition, a common Point-of-Sale V.22 Fast Connect Handshake Protocol (with transparent HDLC) requires these additional settings:

AT+MS=V22	V22 Protocol
AT:U7A,3	Set Fast Connect, Transmit HDLC Flags instead of Marks during hand-shake negotiation.

With either of the Synchronous Access Submodes, once a connection has been established, payload data is multiplexed with command / indicator information by use of <EM> shielding. With <EM> shielding, either of the two bytes <0x19> or <0x99>, used to represent <EM>, precedes a special command, or special indicator.
Note that the Synchronous Access Mode <EM> shielding is designed to support XON/XOFF handshaking. As such, the bytes 0x13 and 0x11 (XON/XOFF) are considered to be special characters in the same way the 0x19 and 0x99 bytes, used for <EM>, are special.
Since the payload data is multiplexed with <EM> shielded command/indicator and possibly XON/XOFF characters, Transparency <EM> codes are defined for the purpose of allowing the host software to send 0x13, 0x11, 0x19 and 0x99 bytes to/from the DCE. For example, if the desire is to send one <0x99> character as a payload character, the host software sends <EM><0x76> instead.
For a complete set of the <EM> command/status see "EM In-band Commands and Status".

Command/Indicator pair	**Hex Code**	**Transmit Direction**	**Receive Direction**	**Supported in**	**Supported in Framed**

				Transparent submode	Submode
<EM><t1>	0x5C	Transmit one 0x19 byte	Received one 0x19 byte	Yes(Note 1)	Yes(Note 1)
<EM><t2>	0x76	Transmit one 0x99 byte	Received one 0x99 byte	Yes(Note 1)	Yes(Note 1)
<EM><t3>	0xA0	Transmit one 0x11 byte	Received one 0x11 byte	Yes(Note 1)	Yes(Note 1)
<EM><t4>	0xA1	Transmit one 0x13 byte	Received one 0x13 byte	Yes(Note 1)	Yes(Note 1)
<EM><t5>	0x5D	Transmit one 0x19 byte	Received one 0x19 byte	Yes	Yes
<EM><t6>	0x77	Transmit one 0x99 byte	Received one 0x99 byte	Yes	Yes
<EM><t7>	0xA2	Transmit one 0x11 byte	Received one 0x11 byte	Yes	Yes
<EM><t8>	0xA3	Transmit one 0x13 byte	Received one 0x13 byte	Yes	Yes
<EM><t9>	0xA4	Transmit 0x19, 0x99	Received 0x19, 0x99	Yes	Yes
<EM><t10>	0xA5	Transmit 0x19, 0x11	Received 0x19, 0x11	Yes	Yes
<EM><t11>	0xA6	Transmit 0x19, 0x13	Received 0x19, 0x13	Yes	Yes
<EM><t12>	0xA7	Transmit 0x99, 0x19	Received 0x99, 0x19	Yes	Yes
<EM><t13>	0xA8	Transmit 0x99, 0x11	Received 0x99, 0x11	Yes	Yes
<EM><t14>	0xA9	Transmit 0x99, 0x13	Received 0x99, 0x13	Yes	Yes
<EM><t15>	0xAA	Transmit 0x11, 0x19	Received 0x11, 0x19	Yes	Yes
<EM><t16>	0xAB	Transmit 0x11, 0x99	Received 0x11, 0x99	Yes	Yes
<EM><t17>	0xAC	Transmit 0x11, 0x13	Received 0x11, 0x13	Yes	Yes
<EM><t18>	0xAD	Transmit 0x13, 0x19	Received 0x13, 0x19	Yes	Yes
<EM><t19>	0xAE	Transmit 0x13, 0x99	Received 0x13, 0x99	Yes	Yes
<EM><t20>	0xAF	Transmit 0x13, 0x11	Received 0x13, 0x11	Yes	Yes
<EM><mark>	0xB0	Begin Transparent Mode	Abort Detected in Framed Submode	Yes	Yes, Receive only
<EM><flag>	0xB1	Transmit a flag; enter Framed Submode if currently in Transparent Submode. If +ESA[E]=1, append FCS to end of frame before sendingclosing HDLC flag.	Detected a non-flag to flag transition. Preceding data was a valid frame. If +ESA[E]=1, sent FCS matches that of the calculated CRC.		Yes
<EM><err>	0xB2	Transmit an Abort	Detected a non-flag to flag transition. Preceding data is not a valid frame.		Yes
<EM><under>	0xB4	not applicable	Detected Transmit Data Underrun	Yes	Yes
<EM><tover>	0xB5	not applicable	Detected Transmit Data Overrun	Yes	Yes
<EM><rover>	0xB6	not applicable	Detected Receive Data Overrun	Yes	Yes
<EM><resume>	0xB7	Resume after a data underrun or overrun (applicable if +ESA[C] = 1)	not applicable		Yes
<EM><bnum>	0xB8	not applicable	<octnum0><octnum1> specifies number of octets in the transmit data buffer if +ITF[C] is non-zero. See Note 2.	Yes	Yes
<EM><unum>	0xB9	not applicable	<octnum0><octnum1> specifies number of discarded octets following a data overrun/underrun, after the <EM><resume> command. This is applicable if +ESA[C] = 1. See Note 2.		
<EM><eot>	0xBA	Terminate carrier, return to command mode.	Loss of carrier detected, return to command mode	Yes	Yes
<EM><ecs>	0xBB	Escape to On-Line command mode	Confirmation of Escape to On-Line command mode.	Yes	Yes
<EM><rrn>	0xBC	Request rate renegotiation	Indicate rate renegotiation	Yes	Yes
<EM><rate>	0xBE	not supported	Retrain/Rate Reneg completed, following octets <tx><rx> indicate tx and rx rates. 0x20 - 1200 bps 0x21 - 2400 bps 0x22 - 4800 bps 0x23 - 7200 bps 0x24 - 9600 bps 0x25 - 12 Kbps 0x26 14.4 Kbps 0x27 - 16.8 Kbps 0x28 - 19.2 Kbps	Yes	Yes

Copyright Delta Design BVBA

			0x29 - 21.6 Kbps 0x2A - 24 Kbps 0x2B - 26.4 Kbps 0x2C - 28.8 Kbps 0x2D - 31.2 Kbps 0x2E - 33.6 Kbps		
Notes: **1.** U87[10] = 1 Can be used to limit the transparency characters in the receive direction, to these four cases only. **2.** The actual value represented in <octnum0><octnum1> = (octnum0 / 2) + (octunum1 x 64) **3.** <EM><Qx45> indicates that an unrecognized <EM> command was sent to the modem.					

Given the example initialization settings shown above, after an ATDT command has been sent to establish a connection, the modem responds with the following.
ATDT12345
CONNECT 1200
PROTOCOL: NONE
<0x19> <0xBE> <0x20> <0x20> <0x19> <0xB1>
The first <EM><rate> indicator shows that the modem connected with a TX rate of 1200 bps, and an RX rate of 1200 bps. The <EM><flag> that occurs immediately after the <EM><rate> indicates that a non-flag to flag transition has occurred, and that the receiver has now been synchronized. Note that an <EM> <flag> indicator is applicable only to the only first occurrence of a non-flag to flag transition. Future occurrences of non-flag to flag transitions are indicated with an <EM> <err> instead. Also, this feature is unique to the U87[8]=1 option. Also note that with U87[8]=1, the Framed Submode is entered immediately upon connection. Otherwise, if U87[8]=0, the Transparent Submode is entered instead, and the host is expected to send an <EM> <flag> to switch to the Framed Submode. After a connection has been established, the modem is ready to transmit and receive frames. For example, if it is desired to send a frame whose contents is:
<0x10><0x11><0x12><0x13><0x14> <0x15>
The host software sends this:
<0x10><0x19><0xA0><0x12><0x19><0xA1><0x14 ><0x15><0x19><0xB1>
Note that the bytes <0x11> and <0x13> are <EM> shielded because these bytes could have been used for XON / XOFF handshaking. In this example, CTS/RTS hardware handshaking is used, so, strictly speaking, it is also possible for the host to have sent this series of bytes instead:
<0x10><0x11><0x12><0x13><0x14><0x15><0x19 ><0xB1> However, if the host chooses not to <EM> shield the 0x11 and 0x13 characters, XON / XOFF software handshaking can no longer be used.
In either of the above transmit frames, the <EM> <flag> is used to indicate that a logical frame has completed.
The modem does not begin transmitting the frame at the DCE until the <EM> <flag> is received, or if the number of bytes sent to the modem exceeds the number of bytes programmed into U87[7:0].
In the above example, the transmission:<0x10><0x19><0xA0><0x12><0x19><0xA1><0x14><0x15><0x19><0xB1>
meets BOTH the criteria of having 10 bytes received atthe DTE, and receipt of an <EM> <flag> command. In this example, the transmission at the DCE begins approximately after the receipt of the <0xB1> byte.
Once an HDLC frame begins transmitting at the DCE, the host must ensure that transmit overruns and underrun do not occur. It is expected that the +ITF command be used to adjust the transmit flow control thresholds so that it is tuned to the system's ability to process the interrupt.
If a transmit underrun occurs, the <EM> <tunder> indicator always appears in the receive path, regardless of how +ESA[C] is programmed.
If +ESA[C] = 0, the modem transmits an abort character at the DCE, at the point of the transmit underrun.
Additional transmit frames can then be transmitted normally.
If +ESA[C] = 1, the modem transmits an HDLC flag at the point of the transmit underrun, and the DCE continues to send only HDLC flags until the host sends an <EM> <resume> command. The <EM> <resume> is then followed by the <EM> <unum> command so that the host software can correct this problem.
A transmit overrun if the host does not properly implement transmit flow control. When a transmit overflow occurs, the <EM> <tover> indicator always appears in the receive path. A transmit overflow is considered to be a catastrophic failure, and results in non-deterministic behavior at the DCE. It is recommended that the session be terminated immediately.
It is expected that the <EM> <tover> and <EM> <tunder> indicators be encountered during system debug, and designing the system software properly to avoid having these indicators occur should be the design goal.
In the receive direction, assuming that the remote modem is another SMD2457L/34/15, this is the expected sequence at the remote receiver DTE, representing the frame sequence of
<0x10><0x11><0x12><0x13><0x14> <0x15>.
<0x10><0x19><0xA0><0x12><0x19><0xA1><0x14 ><0x15><0x19><0xB1>
In the receive direction, the <EM> <flag> indicates that the CRC check is successful, and that the preceding frame. If there had been an error in preceding frame, the <EM> <err> would have been sent instead of the <EM> <flag>. The host is expected to discard the entire frame based on whether or not the frame is terminated with an <EM> <flag> or <EM> <err>. The host should also expect to occasionally see the <EM> <mark> indicator if the sending modem experienced a transmitter underrun or overrun problem.
In general, the RTS flow control is not used. However, if it is used, and if RTS is negated for too long of a time, eventually, the receive buffers will overflow. This is called a receiver overrun, and the modem sends an <EM> <rover> indicator. A receiver overrun is considered to be a catastrophic failure and the host is expected to terminate the session. Host software must be designed so that an <EM> <rover> indicator does not occur.
It is expected that the <EM> <rover> indicator be encountered during system debug, and designing the system software properly to avoid having these indicators occur should be the design goal.
Please note that there is an option available in the U87[10]. The reason for this option is to determine what the modem sends to the DTE when the modem receives back-to-back occurrences of the special characters 0x19, 0x99, 0x11 and 0x13 at the DCE.
As an example, let's say that the following string is received at the DCE:

Copyright Delta Design BVBA

<0x19> <0x19> <0x11> <0x11>
If U87[10] = 0, this is what the host software will receive at the DTE:
<0x19> <0x5D> <0x19> <0xA2>
If U87[10] = 1, this is what the host software will receive at the DTE:
<0x19> <0x5C> <0x19> <0x5C> <0x19> <0xA0> <0x19> <0xA0>
The choice of how to program U87[10] is based on whether or not it is desired to simply the host receive parsing algorithm, or to guarantee that the receive throughput is not overly affected by the <EM> <shielding>. At the very worse case, if there is a large frame consisting only of special characters, the required throughput at the DTE will have to be at least 2x that of the DCE rate to account for the <EM> shielding overhead.
There are two methods of ending a call. One way is to use the <EM> <eot> command, followed by an ATH.
Note that sending the <EM> <eot> command will cause the modem to go to command mode and stop the transmitter, however, the modem does not go back on hook until the ATH.
The other method is to use the <EM> <ecs> command to escape to command mode, and then issue an ATH command. The main difference being that the <EM> <ecs> does not shut off the transmitter. The <EM> <ecs> can also be followed by an ATO command if it is desired that the connection be resumed.

Copyright Delta Design BVBA

5.5 ESCAPE METHODS

There are four ways to escape from data mode and return to command mode once a connection is established. Three of these, "+++", "9th Bit", and the "Escape Pin", allow the connection to be maintained while one or both modems are in the command mode.
These three escape methods can be concurrently enabled, and any enabled escape method functions.
For example, if "+++" and the "Escape Pin" are both enabled, either returns the modem to the command mode from the data mode. The fourth escape method is to terminate the connection.
Always wait for the "OK" before entering the next command after an escape. When making a new connection, do not try to escape between the connect message and the protocol message. An escape attempt in this interval may fail because the modem is not in data mode until after the protocol message.

5.5.1 "+++" Escape

The "+++" escape is enabled by default and is controlled by U70[13] (TES). There are equal guard time periods before (leading) and after (trailing) the "+++" set by the S-Register S12, during which there must be no UART activity. If this UART inactivity criterion is met, the SMD2493L/57/34/15/04 escapes to the command mode at the end of the S12 time period following the "+++". Any activity in the UART during either the leading or trailing time period causes the modem to ignore the escape request and remain in data mode.

5.5.2 "9th Bit" Escape

The "9th Bit" escape mode feature is enabled by sending the AT\B6 command through autobaud, which detects a 9th bit space as "9th bit" escape mode. If this escape method is selected, a 1 detected on the ninth bit in a data word returns the modem to the command mode. The 9th bit is ignored when the modem is in the command mode.

5.5.3 "DTR - Escape Pin" Escape

The "Escape Pin" is controlled by U70[15] (HES). This bit is 0 by default, which disables the Escape pin, ESC, (SMD2493L/57/34/15/04). If HES is set to a 1, a high level on SMD2493L/57/34/15/04,DTR, causes the modem to transition to the on-line command mode. The ESC pin status is polled by the processor, and there is a latency before the "OK" is received and the modem is in command mode. Keep the "escape pin" active until the "OK" is received. In the parallel interface mode, the function of the Escape pin is replaced by bit 2 in the Parallel Interface Register 1. Setting bit 2 to a 1 causes the modem to escape to the command mode.

5.6 SLEEP MODE

The SMD2493L/57/34/15/04 can be set to enter a low power sleep mode when not connected and after a period of inactivity determined by the S24 register. The SMD2493L/57/34/15/04 enters the sleep mode S24 seconds after the last DTE activity, the TX FIFO is empty, and the last data is received from the remote modem. The SMD2493L/57/34/15/04 returns to the active mode when there is a 1 to 0 transition on TXD or if an incoming ring is detected. The delay range for S24 is 1 to 255 seconds. The default setting of S24 = 0 disables the sleep timer and keeps the modem in the normal power mode regardless of activity level.

5.7 POWERDOWN

The powerdown mode is a lower power state than sleep mode but is entered immediately upon writing
U65[13] (PDN) = 1. Once in the powerdown mode, the modem requires a hardware reset via the RESET pin to become active.

5.8 RESET/DEFAULT SETTINGS

The modem must be reset after power is stable and prior to the first "AT" command. The reset pin (SMD2493L/
57L/34L15L/04L, pin 24) must be asserted at least 5 ms low to adequately reset the on-chip registers.
CTS must remain at a Logic 1 (high state) during Reset. The internal pull-up resistor is adequate for most applications. If leakage or transients are present on CTS during Reset, the high value internal resistor should be supplemented with an external 10 k resistor to VCC .

The reset recovery time (the time between a hardware reset or the carriage return of an ATZ command and the time the next AT command can be executed) is approximately 300 ms.
When reset, the SMD2493L/57/34/15/04 reverts to the original factory default settings. Any set-up or configuration data and software updates must be reloaded after every reset. This is true whether the reset occurs due to a power-down/powerup cycle, a power-on reset through a manual reset switch,by writing U6E[4] (RST) = 1, or executing ATZ. A suggested reset sequence is as follows:
1. Apply reset pulse to RESET (SMD2493L/57/34/15/04, pin 24);
write RST bit or ATZ<CR>.
2. Wait > 300 ms.
3. Load firmware updates (if required).
4. Set non-default DAA interface parameters—DCV, ACT, ILIM, OHS2, OHS, RZ, RT, (U67), LIM, (U68).
5. Set non-default cadence values—Busy Tone, Ringback, Ring.
6. Set non-default frequency values—Ring.
7. Set non-default filter parameters.

Copyright Delta Design BVBA

8. Set non-default S-register (values).
The modem is now ready to detect rings, answer another modem, call, or dial out to a remote modem.
Some key default settings for the modem after reset or powerup include the following:

- ♦ V.90 and fall-backs enabled (SMD2457L).
- ♦ V.34 and fall-backs enabled (SMD2434L).
- ♦ V.32bis and fall-backs enabled (SMD2415L).
- ♦ V.22bis and fall-backs enabled (SMD2404L).
- ♦ 42/42bis enabled.
- ♦ "+++" escape sequence enabled.
- ♦ Answer-on-ring is disabled.
- ♦ Speaker off.
- ♦ DTE echo enabled.
- ♦ Verbal result codes enabled.
- ♦ CTS only enabled.
- ♦ FCC (US) DAA and call progress settings.

Review the AT commands and register lists for complete details on all default settings. AT commands and register writes must be used to modify factory defaults after *every* reset, except when the nonvolatile memory is used .

5.9 MEMORY

The user accessible memory in the SMD2493L/57/34/15/04 consists of the S-Registers accessed via the ATSn command, and the U-Registers from 0x0000 to 0x0079 in the main memory space, accessed via the AT:Raa (register read) and the AT:Uaa (register write) commands (where aa is the two digit hexadecimal address of the register).
These memory locations allow the modem to be configured for a wide variety of functions and applications and for global operation.

5.9.1 Firmware upgrades

The SMD2493L/57/34/15/04 contains an on-board Program ROM that includes the firmware required for the features listed in the data sheet. Additionally, the SMD2493L/57/34/15/04 contains on-board Program RAM to accommodate minor changes to ROM firmware. This allows for future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field.
The firmware upgrade, is a file loaded into the SMD2493L/57/34/15/04 Program RAM after a reset using the AT:P command . Once loaded, the upgrade status can be read using the ATI1 command to verify the firmware revision number. The entire firmware upgrade in RAM is always cleared on a reset. To reload the file after a reset or powerdown, the host processor rewrites the file using the AT:P command during post-reset initialization.
A CRC can be run on the upgrade file loaded into on-chip Program RAM with the AT&T6 command to verify that the upgrade was correctly written to the on-chip memory. The CRC value obtained from executing the AT&T6 command should match the CRC value provided with the upgrade code. The following memory notation conventions are followed in this document:
♦ Single variable U-Registers are identified in this document as the register type (i.e., U) followed by the last two digits of the register's hexadecimal address and finally the register "name" in parenthesis. Example: U4A(RGFD). Once the full register reference is made, continuing discussion refers to the register name to simplify the text. The address and value of a single variable U-Register are *always* read from or written to the SMD2493L/57/34/15/04 in hexadecimal.
♦Bit-mapped U-Registers are identified in this document at the top level as the register type (i.e.,U) followed by the last two digits of the register's hexadecimal address and finally the register "name" in parenthesis. Example: U67 (ITC1). Once the full register reference is made, continuing discussion of the register at the top level refers to the register name to simplify the text. The address and value of a bit-mapped U-Register is *always* read from or written to the SMD2493L/57/34/15/04 in hexadecimal.
♦Bits within bit-mapped registers are identified in this document as the register type (i.e., U) followed by the last two digits of the register's hexadecimal address, the bit or bit range within the register in brackets, and finally the bit or bit range "name" in parenthesis. Example: U67[6](OHS) or U67[3:2](DCT). Once the full register reference is made, continuing discussion of the bits or bit range refers to the bit or bit range name to simplify the text. The bit or bit range inside the bracket represents the actual bit or bit range within the register. The value of a bit or bit range is presented in binary for clarity. However, the address and value of a bit-mapped U-Registeris *always* read from or written to the SMD2493L/57/34/15/04 in hexadecimal.
♦SMD2493L/57/34/15/04 S-Registers are identified with a decimal address (e.g., S38) and the number stored in an S-Register is also a decimal value.

5.9.2 Firmware patch

Contact Delta Design for available firmware patches

5.10 SMS SUPPORT

Short Message Service (SMS) is a service that allows text messages to be sent and received from one telephone to another via an SMS service center. The SMD2493L/57/34/15/04 provides an interface that offers a great deal of flexibility in handling multiple SMS standards. This flexibility is possible because most of the differences between standards is handled by the host in the data itself. The SMD24XXL performs the necessary modulation of the data and provides two options for message packet structure (protocol 1 and protocol 2 as defined in ETSI ES 201 912). The rest of the data link layer and the transfer layer are defined by the host system.

Copyright Delta Design BVBA

The SMD24XXL uses a V.23 half-duplex modulation to transmit and receive the data over the PSTN. Two packet structures are provided: protocol 1 and protocol 2. Protocol 2 differs from protocol 1 in that a packet is preceded by 300 bits of channel seizure. ETSI ES 201 912 describes the other differences between protocols 1 and 2, but the host processor handles these when structuring the data within the packet.

Protocol 1

	80 bits of mark (constant 1s)	Message

Protocol 2

300 bits of channel seizure (alternating 1's and 0's)	80 bits of mark (constant 1s)	Message

There are four commands that control the behavior of the SMS feature.

AT+FCLASS = 256	Prepares the modem for handling SMS calls.
ATDT;	Goes off hook and returns to command mode. If a phone number is pro-vided, it is dialed prior to returning to command mode.
AT+FRM = 200	Returns to data mode prepared to receive an SMS message.
AT+FTM = 201	Returns to data mode prepared to transmit an SMS protocol 1 message.
AT+FTM = 202	Returns to data mode prepared to transmit an SMS protocol 2 message.

To enable the SMS features on the SMD24XXL, the host must send "AT+FCLASS = 256" to the modem prior to handling an SMS call. The host can then dial or answer an SMS call using the "ATDTxxxx;", where xxxx is the number to be dialed, or "ATDT;" commands, respectively. Note the semi-colon at the end of the command, which places the modem immediately into command mode after dialing and responds with "OK".
The host can then prepare the modem for transmitting or receiving SMS data. To receive protocol 1 or protocol 2 data, the host must send "AT+FRM = 200". This causes the modem to return to data mode silently listening for data from the remote SMS server. If the modem detects a valid protocol 1 or protocol 2 packet, it responds with a "CONNECT" message followed by the SMS message (without channel seizure and mark). When the carrier stops, the modem returns to command mode and responds with "OK". To transmit protocol 1 or protocol 2 data, the host must send "AT+FTM = 201" or "AT+FTM = 202", respectively. This causes the modem to return to data mode and wait silently until data is received from the host processor for transmission. Once data is received from the host, the modem transmits the proper number of channel seizure and mark bits followed by the data it received from the host. After the modem has begun transmitting, it will send marks when it does not have data to send and will continue to do so until the host escapes to command mode.
The content of the data message is entirely up to the host including any checksum or CRC. ETSI ES 201 912 describes two standard data and transfer layers that are commonly used. SMS typically relies on caller identification information to determine if the call should be answered using an SMS device or not. Please refer to the section on caller ID for more information on how to configure the modem for caller ID detection.

5.11 TYPE II CALLER ID/SAS DETECTION

When a call is in progress, the Subscriber Alerting Signal (SAS) tone is sent by the central office to indicate a second incoming call. The central office may also issue a CPE Alert Signal (CAS) after the SAS to indicate that call waiting caller ID (CWCID) information is available. If properly configured, the modem will acknowledge the CAS tone, receive the CWCID data, and perform a retrain.
The SMD24XXL is configured through the +PCW command to toggle the RI pin (+PCW=0), hang-up (+PCW=1), or do nothing (+PCW=2) upon receipt of the SAS tone.
The default is to ignore the SAS tone. The modem, enabled through the +VCID command, will collect caller ID information if +PCW is set to toggle the RI pin. The AT:I command can be used to verify receipt of the SAS and CWCID data. Bit 9 will be set for SAS receipt due to the RI toggle. Bit 4 will be set if CWCID data is received.
The CWCID data is collected using the +VCIDR? command. The data message is displayed in hexadecimal format using ASCII text. The modem will return NO DATA if no caller ID is available. The +VCIDR response is listed below for the following example CWCID message:

```
Date & Time: 09/11 16:21
ICLID Number:512-555- 1234
Calling Name:JOHN_DOE
+VCIDR:
80 20 01 08 30 39 31 31 31 36 32 31 02 0A 35 31
32 35 35 35 31 32 33 34 07 08 4A 4F 48 4E 5F 44
4F 45 40
OK
```

Character Description	Hex Value	ASCII Value
Message Type (MDMF)	80	
Message Length	20	
Parameter Type(Date/Time)	01	
Parameter Length	08	

Month	30 39	09
Day	31 31	11
Hour	31 36	16
Minutes	32 31	21
Parameter Type (Number)	02	
Parameter Type (Number)	0A	
Number	35 31 32 35 35 35 31 32 33 34	5125551234
Parameter Type (Name)	07	
Parameter Length	08	
Name	4A 4F 48 4E 5F 44 4F 45	JOHN_DOE
Checksum	40	

The SAS tone varies between countries and requires configuration of the user registers U9F – UA9. The SAS_FREQ (U9F) register sets the expected SAS tone frequency as shown .The default SAS frequency is 440Hz. The expected cadence is set in the ten cadence registers SAS_CADENCE0 (UA0) through SAS_CADENCE9 (UA9). The even numbered registers (UA0,UA2,etc.) control the time that the tone is expected to be present and the odd numbered registers select the time that the tone must not be present. The values are expressed in 10 millisecond units. For example, a cadence of on 500 ms, off 300 ms then on for 500 ms may be selected by writing 0x32 to UA0, 0x1E to UA1 and 0x32 to UA2. The unused registers should be written to 0. The default cadence setting is UA0 equal to 0x1E and the remaining nine registers are set to zero.

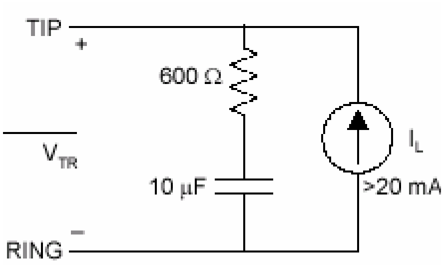
SAS_FREQ (U9F)	SAS Frequency
0	440 Hz (default)
1	400 Hz
2	420 Hz
3	425 Hz
4	480 Hz
5	450 Hz
6	900 Hz
7	950 Hz
8	523 Hz
9	1400 Hz

5.12 TESTING

This section contains information about using the SMD24XXL built-in self-test features and suggestions for board-level testing and presents special test commands.

Self Test

The SMD24XXL advanced design provides the system manufacturer with increased ability to determine system functionality during production tests and to support end-user diagnostics. In addition to local echo, a loopback mode exists allowing increased coverage of system components. For the loopback test mode, a line-side power source is required. While a standard phone line can be used, the test circuit as shown in the figure below is adequate.



The AT&Tn command, in conjunction with the AT&Hn command, performs a loopback self test of the modem. AT&Hn determines the modulation used for the test (V.22bis, V.32bis, etc). If an AT&Hn command is not issued just prior to the start of the test, the default or previously-selected modulation is used.
The test is started with an AT&T2 or AT&T3 command. During the test, the modem is in data mode. To end the test, you must escape data mode using one of the “Escape” methods, such as “+++”, and end the test with AT&T0. The AT&T2 command initiates a test loop from the DSP through the DAA interface circuit of the modem

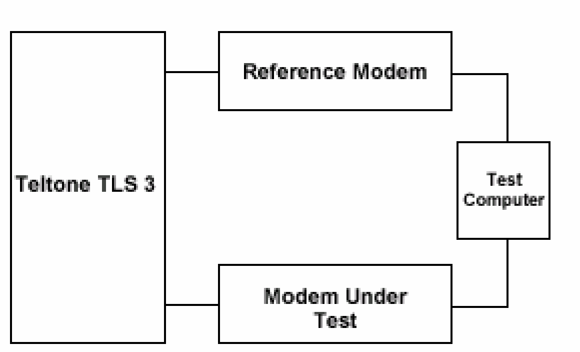
Transmit data is returned to the DSP through the receive channel. AT&T2 tests only the Si2493/57/34/15/04 chip, not the Si3018/10. The AT&T3 command initiates a test loop from the DSP through the DAA interface, the ISOcap™ interface, the Si3018/10, and the hybrid circuit. This test exercises the Si2493/57/34/15/04, the Si3018/10, and many of the external components. A phone line termination with loop current and no dial tone is required for this test since it

Copyright Delta Design BVBA

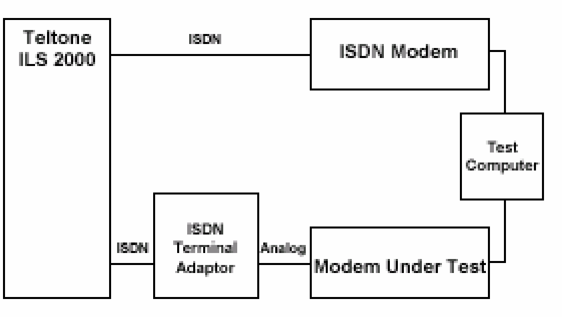
involves the line-side chip (Si3018/10) and the hybrid. The modem is off-hook during this test. The AT&T3 mode is useful during emitted and conducted radiation testing. Set U62(DL) [1] = 1, and issue the AT&T3 command to test the ISOcap link only. The AT\U command is also useful as a production test.
This command places a 25 ms low pulse on RI (SMD24XXL pin 36) and DCD (SMD24XXL pin 39). It also makes INT (SMD24XXL pin 37) the inverse of ESC (SMD24XXL pin 40) and CTS (SMD24XXL, pin 38) the inverse of RTS (SMD24XXL, pin 33). Sending the AT\U command can be used to verify the connection of these pins to the circuit board. This command is terminated by resetting the modem.

Board Test
The modem comes from Delta Design 100% functionally

Functional testing can be used to test special features, such as intrusion detection, caller ID, and overcurrent detection. An intrusion can be simulated by placing a 1 k Ohm resistor across TIP and RING through a relay Caller ID testing requires special test equipment. Many manufacturers choose to use built-in self-test features, such as the &T3 Loopback test described above. Others do a complete functional test of the modem by originating and answering a call and successfully passing a data file in each direction. This process tests the modem and line-side chip functionality, the associated external components, and the software controlling the modem. This test can be done with a modem under test (MUT) and a known-good reference modem or between two modems under test. Testing two modems under test at once reduces test and setup time. Modem operational testing is time consuming and adds to product cost. It is up to the manufacturer to determine whether operational testing is warranted.
Analog modems (Bell 103 through V.34) can be tested by connecting the modems through a telephone line simulator, such as Teltone TLS-3. A call can be placed or received in either direction at the speed set in the modems. A test script must be written for a computer to control the dialing, monitor the call progress, send a file, and compare the received and sent file. The figure illustrates this test configuration.



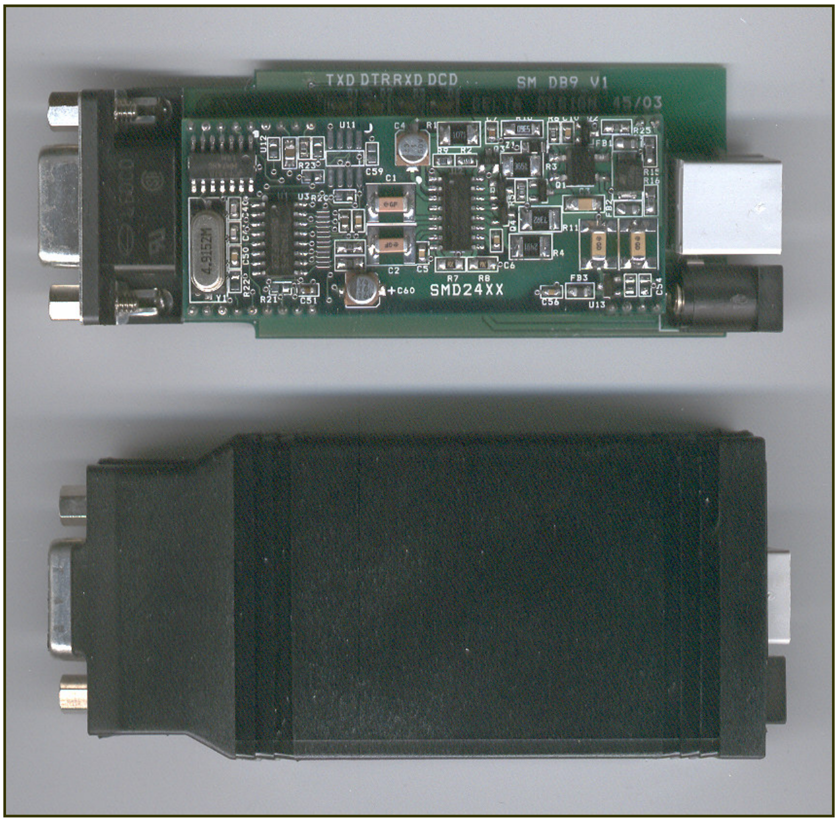
V.90 modems must be tested with a digital modem, such as the USR Courier I. If you do not use a digital modem , the highest connect speed a V.90 modem will support is 33.6 kbps. A call
can be placed or received in either direction at the speed set in the modems. A test script must be written for a computer to control the dialing, monitor the call progress, send a file, and compare the received and sent file.



Copyright Delta Design BVBA

6 EVALUATION

A modem evaluation board (SMD_EV) is available which allows the user to connect the modem module to a PC host via a DB9 cable and to the telephone network via a standard RJ11 cable
The evaluation board fits in a standard plastic housing which allows the modem to be used as a table top modem.



7 ENVIRONMENT

Temperature: 0°C to 50°C
Humidity: 10% to 75% non -condensing

8 DECLARATION OF CONFORMITY

The undersigned hereby declares, that the product SMD24XXL conforms to the main requirements and normative documents according to the Council Directive 1995/5/EEC (R&TTE Directive)

The qualification of the product to requirements is shown by conformance with the following standards

Telecom

ETSI TS103021-1 V1.1.1 (2003-08)
ETSI TS103021-2 V1.1.2 (2003-09)
ETSI TS103021-3 V1.1.2 (2003-09)

Safety

IEC60950-1

EMC

EN55022
EN55024

Copyright Delta Design BVBA

9 CONTACT

DELTA DESIGN BVBA
TIENSESTEENWEG 45
3360 KORBEEK-LO
BELGIUM
TEL: +32 16 461575
FAX: +32 16 461595
info@delta-design.be

The information in this document are subject to change without notice.

Copyright Delta Design BVBA